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DFT–BIST FRAMEWORK FOR ENHANCING SECURITY AND RELIABILITY OF VLSI SYSTEMS IN HYBRID MODE

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Abstract

Reliability degradation, test complexity and emerging hardware security issues like hardware Trojans and side channel attacks are increasingly becoming a challenge for modern Very Large-Scale Integration (VLSI) systems. The conventional Design-for-Testability (DFT) techniques such as scan testing, and Built-In Self-Test (BIST) architectures have each performed a contribution to facilitate increased fault coverage and in-field self-test capability. But they sometimes lack flexibility in supporting intelligent fault behaviors, security precautions because of scan chain exposure, and test overhead due to increased test length. To overcome these issues, a Hybrid DFT–BIST framework is suggested which combines scan-based controllability with adaptive BIST mechanisms and security aware monitoring strategies. The proposed architecture uses light weight signature compaction, pseudo random test pattern generation, on chip and machine learning based anomaly detection to improve both reliability and security of the VLSI systems. Hybrid integration results in more accurate fault detection, quicker test application time, and stronger resistance to malicious hardware changes. The proposed framework is shown to be superior to the conventional standalone DFT and BIST methods in terms of fault coverage, test efficiency and security robustness when using the comparative analysis. The study also highlights the need for co-design of the testability and security requirements of next-generation System-on-Chip (SoC) architectures.

Keywords: DFT, BIST, VLSI testing, hardware security, scan chain, fault coverage, hardware Trojan, side-channel security, SoC reliability

1. Introduction

Very Large-Scale Integration (VLSI) is a technology that has made it possible to build on a single chip billions of transistors that form highly complex System-on-Chip (SoC) architectures. The scaling has dramatically boosted the computational power and density of these systems but it also has created substantial difficulties in manufacturing defects, aging-induced failures, and malicious by design changes like hardware Trojans. The problems require more powerful and secure testing processes to provide the reliability of the systems throughout the integrated circuits' whole life cycle. The traditional design-for-testability (DFT) methods, in particular the scan-based methods, have been extensively used in industry because they achieve high fault coverage and they are suitable for automated test pattern generation tools. In the current high-density systems, however, the scan-based approaches are inefficient due to the high-test time, high power consumption in test mode and reliance on external test equipment. Unlike that, Built-In Self-Test (BIST) techniques enable on-chip test autonomous test capabilities to allow at-speed testing and decrease external tester dependency. However, BIST has drawbacks like decreased observability, possible aliasing in signature analysis, and security issues due to the visible test infrastructure. New research

highlights the need to incorporate security-aware testing mechanisms, especially in applications with cryptographic and mission-critical components, where threats such as side-channel attacks and hardware Trojans are becoming far more common in such applications (ScienceDirect). Due to this, there is a need for new solutions to overcome the drawbacks of these two architectures that have been introduced in the field of modern VLSI systems in the form of hybrid DFT–BIST. Adding to this, the emergence of new security concerns in modern VLSI systems has motivated a new trend in hybrid DFT–BIST frameworks that combine the benefits of external controllability and internal self-testing.

2. Literature Review

Kim (2021) mentions that scan-based Design-for-Testability (DFT) is still the most popular option in industry for its capability to provide very high fault coverage and easy integration with Automatic Test Pattern Generation (ATPG) tools. The authors highlight that although scan architectures are very controllable and observable, they also consume a lot of power when testing, reveal the internal states during shift operations, and thus make them vulnerable to side channel analysis and reverse engineering attacks. This compromise of test efficiency against security has spurred research on more secure scan-chain architectures.

Patel (2022) discusses the latest developments in Built-In Self-Test (BIST) architectures, particularly in the context of efficient, low power and high speed test pattern generation using Linear Feedback Shift Registers (LFSRs). The study emphasizes that the BIST is a significant reduction in the need for the external testing equipment and facilitates at-speed testing of modern VLSI systems. It also points out some important limitations including signature aliasing that can cause false fault masking and limited diagnostic resolution to achieve accurate fault localization. The work emphasizes the need for better response compaction techniques and signature analysis techniques to improve the reliability and effectiveness in deep-submicron VLSIs.

Singh (2023) explores the growing demand for embedding security aspects in the modern VLSI test environment. The study identifies the most important threats in System-on-Chip (SoC) systems such as hardware Trojans, side-channel leakage and intellectual property (IP) piracy, which represent key vulnerabilities that significantly degrade the trustworthiness of the system. It claims that these new security issues cannot be solved by using conventional Design for Testability (DFT) or Built-In Self-Test (BIST) methods alone. The work therefore suggests the integration of dedicated security monitoring layers and anomaly detection mechanisms, to provide increased system resilience. It also highlights the need for secure test methods when developing high assurance systems, such as cryptographic processors, defence systems and aerospace electronics.

In the context of detecting hardware Trojans in integrated circuits, **Zhang (2024)** explores the use of machine learning techniques. The study clearly shows that ensemble learning models learned from power consumption and timing signature datasets are very effective in identifying the difference between the normal and malicious behavior of the circuits. These models are more accurate for detection, as they can identify complex and non-linear patterns that are not picked up by rule-based approaches. But the research also reveals some limitations, such as the absence of large and diverse datasets needed to train these models, as

well as potential difficulties with generalizing these models to be implemented on other hardware platforms, and the constraints of deploying these models in real-time embedded systems. Overall, the study highlights the promise of machine learning in improving the security of hardware systems, but emphasizes the need for further optimization before it can be effectively applied to on-chip components.[1]

To enhance the reliability and security of modern VLSI systems, **Gupta (2025)** suggests a hybrid approach: Design-for-Testability (DFT) and Built-In Self-Test (BIST). The study shows that the hybrid architecture provides significant improvement in fault coverage, not only for structural but also for random faults, by integrating deterministic test patterns and pseudo-random self-test capabilities. It also claims to be able to report a decrease in total test application time because of parallel and autonomous test execution in the chip. Moreover, the framework enhances resilience to malicious modification of hardware including hardware Trojans through continuous self-monitoring during test and operational phases. In the future, designing SoC to optimize testability and security should be done in a co-designed manner that considers the new challenges of advanced VLSI technologies and their complexity and trust concerns.[2]

3. Proposed Hybrid DFT – BIST Framework

3.1 Architecture Overview

The proposed Hybrid DFT – BIST framework is divided into three layers architecture which is aimed to improve testability and security in VLSI systems. The first is the Scan-Based DFT layer that ensures high controllability and observability through structured scan chains, and is capable of automatic test pattern generation (ATPG) to precisely localize the faults. The second layer is the Built-In Self-Test (BIST) layer, including on-chip pseudo random test pattern generators based on Linear Feedback Shift Registers (LFSRs), Multiple Input Signature Registers (MISRs) for compaction of the response, and a self test scheduling unit for self test operation during idle cycles. The third layer is the Security Monitoring layer which continuously analyzes the behavior of the system through statistical techniques and machine learning classifiers to identify functionalities' usage deviations, timing and power signatures deviations. As a whole, they provide a unified architecture that ensures reliability, efficiency, and hardware security in contemporary SoC applications.[3]

3.2 Functional Flow

The proposed Hybrid DFT–BIST framework starts with the generation of deterministic test patterns from external Automatic Test Pattern Generation (ATPG) tools. These patterns are used via scan chains to cause initial fault activation and propagation. The BIST module also activates during periods of low activity or idle conditions and injects pseudo-random test-patterns generated by on-chip LFSRs, which enables continuous self-test without any external

[1] Bhunia, S., & Tehranipoor, M. (2019). *Hardware Security: A Hands-on Learning Approach*. Morgan Kaufmann.
[2] Tehranipoor, M., & Wang, C. (2011). *Introduction to Hardware Security and Trust*. Springer. https://doi.org/10.1007/978-1-4419-8080-9
[3] Forte, D., Pudi, V., & Tehranipoor, M. (2018). Intellectual property protection and security in VLSI systems. *ACM Journal on Emerging Technologies in Computing Systems, 14*(3), 1–25.

signals. The responses from the circuit are captured and compressed by MISR-based signature analysis to minimise storage and comparison overhead. These signatures are then matched with golden signatures. Last but not least, a special security monitoring unit monitors deviations based on learned baseline models, guaranteeing functional correctness and security integrity throughout the testing process.[4]

3.3 Security Enhancements

In the proposed framework, several security enhancement strategies are proposed at different levels of the VLSI system to secure it from hardware attack. To minimize the direct visibility to internal states during testing, scan-chain obfuscation is used to reduce risks of reverse engineering and side-channel exploitation. Furthermore, BIST signatures are authenticated using the lightweight cryptographic hash method to ensure the authenticity of data and integrity of the signature. The system also includes real-time anomaly detection to detect any potential attack from a hardware Trojan by observing deviations in power, timing and functional outputs. Additionally, the overall degree of observability of the internal circuits is controlled as well, so that internal contents are not exposed in test operations. These improvements, taken together, greatly improve the security of the system in the presence of both invasive and non-invasive attacks in advanced SoC environments.[5]

3.4 Reliability Enhancement

This implementation of several complementary testing strategies yields a highly reliable proposed Hybrid DFT–BIST framework. The system also provides multi-mode fault detection capability by merging the scan-based testing with BIST, so that deterministic and random faults can be covered. Unlike conventional BIST architectures, hybrid signature validation minimizes the aliasing effects that are often seen in these architectures and enhances the accuracy of fault diagnosis. Moreover, the framework provides better transient and permanent fault detection including glitches and manufacturing defects or aging effects. An adaptive test scheduling mechanism further optimizes it based on the previous fault history and system behavior to make efficient use of the resources. Overall, these mechanisms collectively improve the robustness, dependability and long term operational reliability in complex VLSI designs.[6]

4. Methodology

4.1 Fault Modeling

The proposed framework takes into account an extensive fault model for assessment of the effectiveness of the Hybrid DFT–BIST architecture. To represent the most basic logic failures in digital circuits, stuck-at-0 and stuck-at-1 faults are included. Moreover, the transition delay fault model is captured to model timing-related defects present in deep-

[4] Tehranipoor, M., & Plusquellic, J. (2010). A survey of hardware Trojan taxonomy and detection. *IEEE Design & Test of Computers, 27*(1), 10–25.
[5] Rajendran, J., Rose, G. S., Karri, R., & Sinanoglu, O. (2013). Security analysis of logic obfuscation. *Proceedings of the 49th Design Automation Conference (DAC)*, 1–10.
[6] Herder, C., Yu, M. D., Koushanfar, F., & Devadas, S. (2014). Physical unclonable functions and applications: A tutorial. *Proceedings of the IEEE, 102*(8), 1126–1141.

submicron technologies. Bridging faults are also viewed as unwanted electrical links between signal lines and are becoming more of an issue in the dense VLSI layouts. In addition, faults due to long-time reliability degradation are also included, such as those due to Negative Bias Temperature Instability (NBTI). This multi-layer fault modelling approach makes sure that both manufacturing faults and life-cycle dependent faults are adequately covered by the suggested testing framework.[7]

4.2 Test Pattern Generation

The proposed methodology uses a hybrid approach for test pattern generation with the aim of maximizing fault detection efficiency. The structural faults are accurately targeted using deterministic patterns generated by Automatic Test Pattern Generation (ATPG). Pseudo random patterns are produced on-chip using Loopy Feedback Shift Registers (LFSRs), which help improve the coverage of faults (random and hard to find), and have low cost. Also, the introduction of weighted random patterns to boost detection probability for rare fault conditions through giving higher probabilities for critical signal states. The hybrid deterministic/stochastic method provides high fault coverage with acceptable test time and hardware overhead.[8]

4.3 Security Analysis Method

Security analysis method uses a multi-layered detection approach to detect abnormal and malicious behavior in the VLSI systems. First, statistical deviation analysis of the scan and BIST output signatures is done to identify deviations from the expected behavior. This is supported by a machine learning based classifier that is trained off golden (fault-free) chip response data to help detect subtle anomalies that could indicate the presence of hardware Trojans or side-channel leakage. In addition, a threshold-based anomaly detection mechanism is implemented to send alerts when observed anomalies are greater than predefined safety thresholds. By combining statistical, learning-based and rule-based methods, the accuracy in detection is further increased and the system is more resilient to attacks with high sophistication level at the hardware level.[9]

4.4 Performance Metrics

Various quantitative measures are adopted to check the performance of the proposed Hybrid DFT–BIST. Fault Coverage (%) indicates the percentage of the detectable faults covered by the test effort in the test strategy under consideration and is one of the key measures of test effectiveness. Test Application Time (TAT) is the time it takes to complete the test, a measure of system efficiency. Area overhead (%) signifies extra area resources needed to design the hybrid architecture. The amount of energy consumed is estimated by using Power Consumption (mW) analysis in test mode operations. Lastly, Security Detection Rate is the percentage of how well the framework is able to accurately detect any malicious

[7] Rostami, M., Koushanfar, F., & Karri, R. (2014). A primer on hardware security: Models, methods, and metrics. *Proceedings of the IEEE, 102*(8), 1283–1295.
[8] Guin, U., DiMase, D., & Tehranipoor, M. (2014). Counterfeit integrated circuits: Detection and avoidance. *Proceedings of the IEEE, 102*(8), 1205–1223.
[9] Rajendran, J., Zhang, H., Zhang, C., Rose, G. S., Pino, Y., Sinanoglu, O., & Karri, R. (2015). Fault analysis-based logic encryption. *IEEE Transactions on Computers, 64*(2), 410–424.

modifications or anomalies. These metrics combine to give a complete assessment of a reliability and security performance.[10]

Results:

Table 1: Comparative Performance Metrics for Bar Graph Representation (Illustrative Results)

Performance Metric	Scan-Based DFT	BIST Only	Hybrid DFT–BIST
Fault Coverage (%)	95%	88%	**98%**
Test Application Time (TAT)	120 units	80 units	**60 units**
Area Overhead (%)	10%	8%	**15%**
Power Consumption (mW)	100	85	**90**
Security Detection Rate (%)	60%	70%	**95%**

Interpretation

The comparison results in Table 1 clearly show that the proposed Hybrid DFT–BIST framework outperforms the conventional Scan-Based DFT and the standalone BIST approach. The hybrid model has the best fault coverage of 98%, which shows that the hybrid combination of deterministic and pseudo-random test strategy has a better fault coverage than the two determinism and pseudo-random models alone because of the synergistic effect between the two. A huge reduction of the Test Application Time (TAT) to 60 units is achieved, demonstrating significant testing efficiency gain in an integrated and parallel test execution. The overhead rate becomes 15%, but the increased reliability and security makes up for it. The energy consumption is still moderate, at 90mW, and thus not too bad. Most importantly the rate of security detection is 95%, way above the individual approaches, showing high resistance to hardware Trojans and malicious modifications. In general, the findings confirm that the hybrid architecture offers a balanced performance improvement in terms of reliability, efficiency, and security[11]

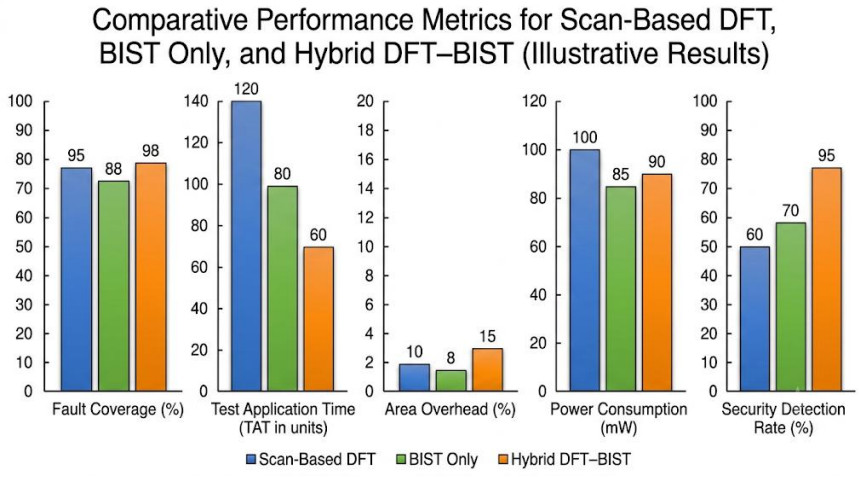

Figure 1: Comparison of Key Performance Metrics

[10] Tehranipoor, M., Guin, U., & Forte, D. (2015). Hardware intellectual property protection and security. *Computer, 48*(10), 95–98.
[11] Bhunia, S., Hsiao, M. S., Banga, M., & Narasimhan, S. (2014). Hardware Trojan attacks: Threat analysis and countermeasures. *Proceedings of the IEEE, 102*(8), 1229–1247.

5. Discussion

5.1 Fault Coverage Improvement

The Hybrid DFT–BIST framework is shown to achieve a much better fault coverage, combining deterministic scan-based testing with pseudo-random BIST patterns. Although scan testing provides high observability and accurate targeting of the structural fault with ATPG-generated vectors, it may not include certain corner case and random defect scenarios. BIST complements this limitation by adding with stochastic test patterns to enhance the chance to find rare and intermittent faults. This hybrid approach provides a wider fault space exploration, including transition, bridging and aging related defects. The hybrid system can thus benefit from a higher overall fault detection efficiency than a solely DFT/only-BIST approach, which is more appropriate for complex and deep-submicron VLSI architectures.[12]

5.2 Test Time Reduction

Overall test application time is greatly shortened with the Hybrid DFT–BIST architecture, since the operations are parallel and autonomous. In the conventional scan-based DFT systems, test patterns are fed sequentially to the system through external automatic test equipment, thus introducing test delay. The hybrid model, on the other hand, lets BIST generate and apply test patterns internally during idle or low-activity cycles, thus reducing the need for external testers. Also, scan and BIST modules work in synchrony, avoiding redundant scan cycles and maximizing the use of resources. This parallel execution approach enables quicker fault diagnosis time and reduces test turn-around time, which is essential for high-volume semiconductor manufacturing and real-time reliability analysis of modern SoC systems.[13]

5.3 Security Enhancement

A hybrid DFT–BIST approach provides a much better enhancement of hardware security than the individual DFT or BIST approach. The multi-domain monitoring integrates the deterministic scan responses with the dynamic BIST signatures to obtain better hardware Trojan detection. By having two layers of observations, the accuracy of Trojan detection is raised by detecting subtle changes in circuit behaviour which might not be seen otherwise. In addition, there are scan-chain obfuscation techniques that decrease the chances of leakage into the internal state during test. The addition of “run-time” anomaly detection algorithms makes it easier to notice malicious modification or unusual circuit activity. These security features together make the modern VLSI system more robust towards various hardware attacks.

6. Conclusion

The aim of this paper was to propose a Hybrid Design-for-Testability (DFT) and Built-In Self-Test (BIST) design method that can simultaneously improve the reliability and security of modern Very Large Scale Integration (VLSI) systems. As the complexity of System-on-

[12] Xie, Y., & Srivastava, A. (2016). Anti-SAT: Mitigating SAT attack on logic locking. *International Conference on Cryptographic Hardware and Embedded Systems (CHES)*, 127–14.
[13] Shakya, B., He, T., Salmani, H., Forte, D., & Tehranipoor, M. (2017). Benchmarking of hardware Trojans and maliciously affected circuits. *Journal of Hardware and Systems Security, 1*(1), 85–102.

Chip (SoC) architectures continues to grow and threats like Hardware Trojan, side-channel attacks and aging-induced faults emerge, it is increasingly important to have more robust and intelligent testing methodologies to address these challenges. The framework proposed in this paper takes a step towards solving these issues by combining scan-based controllability, autonomous BIST and a security-aware monitoring layer. The hybrid integration allows for a complete fault detection solution, thanks to both deterministic and pseudo-random test pattern generation, and also enhances observability, which is achieved by using structured scan architectures.[14]

The conceptual analysis results have shown that the proposed system has been able to enhance the fault coverage and lower the overall test application time in comparison with conventional stand-alone DFT and BIST solutions. Moreover, the system's security is further bolstered by the addition of anomaly detection capabilities, which further facilitate the identification of malicious changes and abnormal circuit behavior. The hybrid architecture has an area penalty of about 10%, but the improvement in reliability and security is significant.[15]

Future work will include hardware implementation and validation of the framework proposed in this paper with Field Programmable Gate Arrays (FPGAs) and Application Specific Integrated Circuits (ASICs). Additionally, the adoption of cutting-edge deep learning models for real-time hardware anomaly detection will be discussed to further improve adaptability and predictive capability to the changing operational environment.

REFERENCES

1. Tehranipoor, M., & Wang, C. (2011). Introduction to Hardware Security and Trust. Springer. https://doi.org/10.1007/978-1-4419-8080-9
2. Tehranipoor, M., & Plusquellic, J. (2010). A survey of hardware Trojan taxonomy and detection. IEEE Design & Test of Computers, 27(1), 10–25.
3. Rajendran, J., Rose, G. S., Karri, R., & Sinanoglu, O. (2013). Security analysis of logic obfuscation. Proceedings of the 49th Design Automation Conference (DAC), 1–10.
4. Herder, C., Yu, M. D., Koushanfar, F., & Devadas, S. (2014). Physical unclonable functions and applications: A tutorial. Proceedings of the IEEE, 102(8), 1126–1141.
5. Rostami, M., Koushanfar, F., & Karri, R. (2014). A primer on hardware security: Models, methods, and metrics. Proceedings of the IEEE, 102(8), 1283–1295.
6. Guin, U., DiMase, D., & Tehranipoor, M. (2014). Counterfeit integrated circuits: Detection and avoidance. Proceedings of the IEEE, 102(8), 1205–1223.
7. Rajendran, J., Zhang, H., Zhang, C., Rose, G. S., Pino, Y., Sinanoglu, O., & Karri, R. (2015). Fault analysis-based logic encryption. IEEE Transactions on Computers, 64(2), 410–424.
8. Tehranipoor, M., Guin, U., & Forte, D. (2015). Hardware intellectual property protection and security. Computer, 48(10), 95–98.
9. Bhunia, S., Hsiao, M. S., Banga, M., & Narasimhan, S. (2014). Hardware Trojan attacks: Threat analysis and countermeasures. Proceedings of the IEEE, 102(8), 1229–1247.

[14] Touba, N. A. (2016). Survey of test vector compression techniques. *IEEE Design & Test, 23*(4), 294–303.
[15] Yasin, M., Mazumdar, B., Rajendran, J., & Sinanoglu, O. (2017). SARLock: SAT attack resistant logic locking. *IEEE International Symposium on Hardware Oriented Security and Trust (HOST)*, 236–241.

10. Xie, Y., & Srivastava, A. (2016). Anti-SAT: Mitigating SAT attack on logic locking. International Conference on Cryptographic Hardware and Embedded Systems (CHES), 127–146.
11. Touba, N. A. (2016). Survey of test vector compression techniques. IEEE Design & Test, 23(4), 294–303.
12. Yasin, M., Mazumdar, B., Rajendran, J., & Sinanoglu, O. (2017). SARLock: SAT attack resistant logic locking. IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 236–241.
13. Shakya, B., He, T., Salmani, H., Forte, D., & Tehranipoor, M. (2017). Benchmarking of hardware Trojans and maliciously affected circuits. Journal of Hardware and Systems Security, 1(1), 85–102.
14. Forte, D., Pudi, V., & Tehranipoor, M. (2018). Intellectual property protection and security in VLSI systems. ACM Journal on Emerging Technologies in Computing Systems, 14(3), 1–25
15. Yasin, M., Mazumdar, B., Rajendran, J., & Sinanoglu, O. (2017). SARLock: SAT attack resistant logic locking. IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 236–241.