  

# High-Speed MAC Unit Design using Sequential Finite-Field Multiplier and Pipelined Adder Architecture for DSP Applications

**Dr. U. Rajender**

Assistant Professor, Department of Electronics and Communication Engineering, Vaageswari College of Engineering, Karimnagar, Telangana

## ABSTRACT

In the realm of digital signal processors (DSPs), there is always a demand for additional processing capacity, particularly when it comes to the incorporation of a greater number of central processing unit cores onto a single integrated circuit. Digital signal processors (DSPs) are capable of performing a wide variety of operations, including convolution, transformation, correlation, and filtering, which essentially need multiplication and repeated addition. The Multiply and Accumulate unit (MAC) is an essential component of digital signal processors (DSPs), which highlights the importance of implementing high-performance operations inside this unit. There is a major dependence on the speed performance of the MAC for DSP algorithms. The implementation of MAC architecture has traditionally been accomplished through the use of bit-parallel computing techniques. However, as bit precision grows, these techniques result in quadratic increases in the amount of hardware that is required. Alternatively, bit-serial computing is a method that serializes a single input in order to make hardware proportionate to bit precision. It reduces the requirements for hardware. Another significant challenge that arises as technology progresses is the dissipation of static power. Based on the Sequential Finite-Field Multiplier (SFFM) methodology, this research provides a high-speed MAC unit that was developed specifically for use in arithmetic applications. When designing the adder blocks that are contained within the MAC unit, the high-speed pipelined adder architecture is something that is utilized.

**Keywords**: Multiply and Accumulate unit, Digital signal processors, Sequential Finite-Field Multiplier, High-Speed Processing, Pipelined Adder.

## 1. INTRODUCTION

When designing a very large scale integrated circuit (VLSI), one of the most typical tasks is designing a multiplier and accumulator utilizing sequential finite field operations. This work is used for a variety of applications, such as cryptography, error correcting codes, and digital signal processing. The design calls for the implementation of sequential circuits that are capable of carrying out arithmetic operations within a domain that is finite. One of the fundamental methods includes encoding the operands and the output as polynomials with coefficients in a finite field, such as the Galois field (GF). After that, the arithmetic operations are carried out on these polynomials by utilizing a variety of algorithms, such as the Karatsuba, Toom-Cook, and Montgomery multiplication algorithms. There are often numerous steps involved in the construction of the multiplier and accumulator. These stages include input and output registers, a finite field arithmetic logic unit (ALU), and pipeline registers for sequential processing. Pipeline registers contribute to the reduction of the critical path delay and the enhancement of the design's throughput with increasing efficiency. The design process begins with the creation of a high-level architecture, which is then followed by the selection of algorithms and their optimization. In the following stage, you will be responsible for developing the finite field ALU and putting it into action by utilizing digital logic gates. After that, a hardware description language (HDL) is used to model the circuit, and then a netlist is generated through the use of electronic synthesis.Tools like as place and route (P&R) and static timing analysis (STA) are utilized in order to optimize the netlist in terms of area, power, and time. Simulations of both the functionality and timing of the design are then used to validate the design. Using sequential finite field operations to construct a multiplier and accumulator is a difficult process that requires a comprehensive understanding of arithmetic algorithms, digital logic design, and VLSI design methodologies. In conclusion, this is a challenging task that requires attention to detail. In order to fulfill the criteria of the application that is being targeted, the design needs to be optimized in terms of area, power, and timing. As an example, encryption, error correcting codes, and digital signal processing are all examples of applications that require the computation of arithmetic operations in finite fields to be performed at a high speed and with efficiency. The use of finite field operations is necessary for the secure encryption and decryption of data, the repair of errors that occur during data transmission, and the processing of signals in communication communication systems. When compared to software-based systems, the implementation of sequential finite field operations employing VLSI technology has the potential to give significant advantages in terms of both performance and power efficiency. Because of this, very large scale integrated circuits are able to take use of the parallelism and pipelining that are inherent in arithmetic operations, which allows them to achieve high throughput and low latency. VLSI circuits are able to be modified to fulfill the particular requirements of the application, which may include specifications about area, power, and performance. The need for high-speed and efficient computation of arithmetic operations in finite fields, combined with the advantages of VLSI technology in achieving high performance and low power consumption, is the impetus behind the design of a multiplier and accumulator that involves sequential finite field operations in very large scale integration (VLSI).

## 2. LITERATURE SURVEY

Sahu, Ajay Kumar (2021)[1], this work investigated existing work and techniques used by several authors to minimize the power consumption in the design of MAC Unit. This review can provides aninsight to the beginners in the VLSI Arithmetic Circuit Design to gain more idea on Low power MAC Unit Design Rishi Kiran , E.Swathi Vangala and J. V. R. Ravindra , In this work , PERAM deals with reversible array multiplier. As it consists of rudimentary reversible gates like CCNOT and CNOT, analysis will be uncomplicated. The proposed design methodology is implemented and verified in cadence© virtuoso of 45 nm technology showing the improvement of 77.76% in terms of power, 71.39% in terms of power delay product. PERAM shows a great variation in the power and power delay product. Gunasekaran, K., et al(2022)[2] ,this work proposed a reversible logic design of a 4-bit MAC structure using Peres gates as reversible logic blocks. In addition, a variety of parameters, along with those of conventional computing, perform a relative test between classical style and quantum logic operation. Priyadarshini, K. Mariya, et al(2021) [3], In this work investigation, Pre-Accumulator and Post-Multipliers (PAPM) are proposed which accelerate the speed of processor. 4-bit multiplier using Carry Save Adder (CSA) is built with 6Transistors-Adder and sutras of Vedic mathematics is constructed. Accumulator of multiplier and accumulator are designed with Two Level Edge Triggering Flip-Flops (TLET-FF) to increase bandwidth of the memory. The proposed architecture of Multiply Accumulate (MAC) circuit consumes very less power when compared to existing high speed MACs. Inayat, Kashif, and Jaeyong Chung(2020) [4], this demonstrated the hybrid accumulator with partial CPA factoring in "Gemmini," an open-source practical systolic array accelerator and factoring technique does not change the functionality of the base design Puttam, HS Krishnaprasad, P. Sivadurga Rao, and N. V. G. Prasad. (2012)[6] , In this work , we proposed a new architecture of multiplier -and-accumulator (MAC) for high-speed arithmetic and low power. Multiplication occurs frequently in finite impulse response filters, fast Fourier transforms, discrete cosine transforms, convolution, and other important DSP and multimedia kernels Sathish, M. V., and Mrs Sailaja(2011)[7] ,in this work a new architecture of multiplier-and accumulator (MAC) for high-speed arithmetic. By combining multiplication with accumulation and devising a hybrid type of carry save adder (CSA), the performance was improved. Since the accumulator that has the largest delay in MAC was merged into CSA, the overall performance was elevated. The proposing method CSA tree uses 1's- complement-based radix-2 modified Booth's algorithm (MBA) and has the modified array for the sign extension in order to increase the bit density of the operands.Teja, Ravi, et al224-230[8] , In this work , we proposed a new architecture of multiplier-and-accumulator (MAC) for high-speed arithmetic. By combining multiplication with accumulation and devising a hybrid type of carry save adder (CSA), the performance was improved. Since the accumulator that has the largest delay in MAC was merged into CSA, the overall performance was elevated. The CSA propagates the carries to the least significant bits of the partial products and generates the least significant bits in advance to decrease the number of the input bits of the final adder.Khubnani, Rashi, Tarunika Sharma, and Chitirala Subramanyam et.al2022[9]. , in this work Vedic Multiplier is a key tool in rapidly growing technology especially in the immense domain of Image processing, Digital Signal Processing, real-time signal. Multipliers are important block in digital systems and play a critical role in digital designs. Along with accuracy demand for minimizing time area, power, and delay of the processor by enhancing speed is the focus point. Vedic mathematics rules and Algorithms generate partial products concurrently and save time. This paper is a review of the application and modification of Vedic multiplier in different fields and a comparison of Vedic multiplier with other multipliers for enhancing performance parameters.Ponugoti, Vamshi, et al(2022)[10] , in this paper presents a four-bit Baugh-Wooley multiplier using full swing gate diffusion input (GDI) technology. In general, addition is a crucial arithmetic operation and is heavily demanded in VLSI design. These are widely used in digital signal processing, accumulators, microprocessors and many other applications. So, the full adder performance decides the overall system performance.N. Pandu Ranga, and K. Maheswari Devi.et.al(2022)[11] , in this work MAC unit performed important operation in many of the digital signal processing (DSP) applications. In existing method the multiplier is designed using modified Wallace multiplier and the adder is done with carry save adder. Nithiya, C., et al(2022)[12]. in this test bench work the proposed approach uses the RADIX-4 and RADIX-8 models with a glitch optimization circuit to construct a low power adjustable path selective Booth Multiplier architecture. The system utilized low power techniques like clock gating and sequenced latching process. The design is simulated using Modelsim tool and validated with test and evaluation of multiplier circuit with equivalent test bench.

## 3. PROPOSED METHODOLOGY

MAC is composed of an adder, multiplier, and an accumulator. Usually adders implemented are Carry- Select or Carry-Save adders, as speed is of utmost importance in DSP. One implementation of the multiplier could be as a parallel array multiplier. The inputs for the MAC are to be fetched from memory location and fed to the multiplier block of the MAC, which will perform multiplication and give the result to adder which will accumulate the result and then will store the result into a memory location. This entire process is to be achieved in a single clock cycle. The architecture of the MAC unit which had been designed in this work consists of one 16 bit register, one 16-bit Modified Booth Multiplier, 32-bit accumulator. To multiply the values of A and B, Modified Booth multiplier is used instead of conventional multiplier because Modified Booth multiplier can increase the MAC unit design speed and reduce multiplication complexity. SPST Adder is used for the addition of partial products and a register is used for accumulation. The operation of the designed MAC unit is as in Figure 1. The product of Ai X Bi is always fed back into the 32-bit accumulator and then added again with the next product Ai x Bi. This MAC unit is capable of multiplying and adding with previous product consecutively up to as many as times.

### 3.2 Sequential Finite Field Adder

Adder–subtractor tree is a useful sub–circuit that often finds applications in the parallel implementation of distributed arithmetic-based FIR Filters, matrix multiplication circuits or pipelined binary tree multipliers. Each ADD/SUB block shown in Figure 2 can be independently configured as a two’s complement adder or subtractor, as they have independent mode select lines. Each of the blocks can perform a 24–bit two’s complement addition/subtraction, with a total of five stages of ADD/SUB blocks. The circuit has also been redesigned by inserting scan FFs at the site of the pipeline registers with no hardware overhead and performance deterioration. The slice configuration of a pipelined adder/subtractor tree without the scan FFs have been shown in Figure 3.

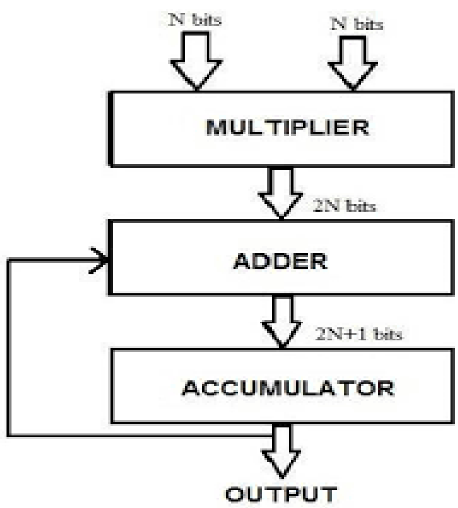


Fig.1.Multiplier and Accumulator Architecture

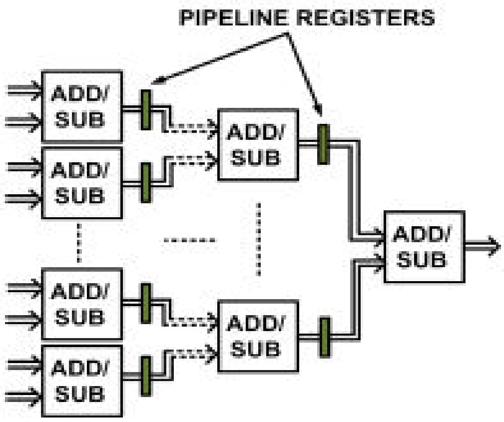


Figure 2. Block diagram of pipelined adder subtractor tree

The sum bit can be computed by EX–ORing the LUT and carry chain multiplexer output as Si = Ai ⊕ (Bi ⊕ M) ⊕ Ci. The carry output of each multiplexer stage can be computed as**:**

$$\begin{aligned} C_{i+1} &= A_i(B_i \oplus M) + (A_i \oplus (B_i \oplus M))C_i \\ &= A_i(A_i(B_i \oplus M) + \overline{A_i}(\overline{B_i \oplus M})) \\ &\quad +(A_i \oplus B_i \oplus M)C_i \\ &= A_i(A_i \odot (B_i \oplus M)) + (A_i \oplus B_i \oplus M)C_i \end{aligned}$$

**Sequential Finite Field Multiplier:** Sequential Finite Field multiplier is the simplest structure of parallel multiplier. This multiplier using the standard adds and shift operation based on 'add and shift' algorithms to perform a multiplication operation. The structure of 4-bit array multiplier is presented in fig. 6. The partial products generator consists of n number of 'AND' gates to multiply the multiplicand with each bit of the multiplier and then these partial products are shifted depending on their order and this summation operation can be performed by using full adder and a half adder. In 4x4 Sequential Finite Field Multiplier, 4x4 AND gates used to generate partial products and 4x (4-2) full adders, and 4 half adders used to generate.

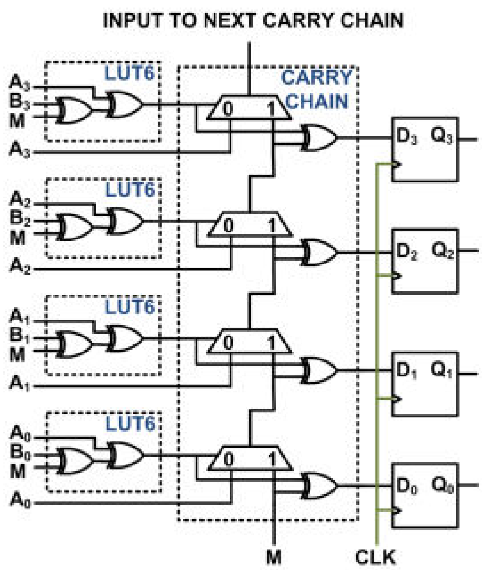


Figure 3. Original pipelined adder subtractor design

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## 4. RESULTS AND DISCUSSION

The simulation results are done using in VIVADO ISE. The timing, power and synthesis reports listed below.

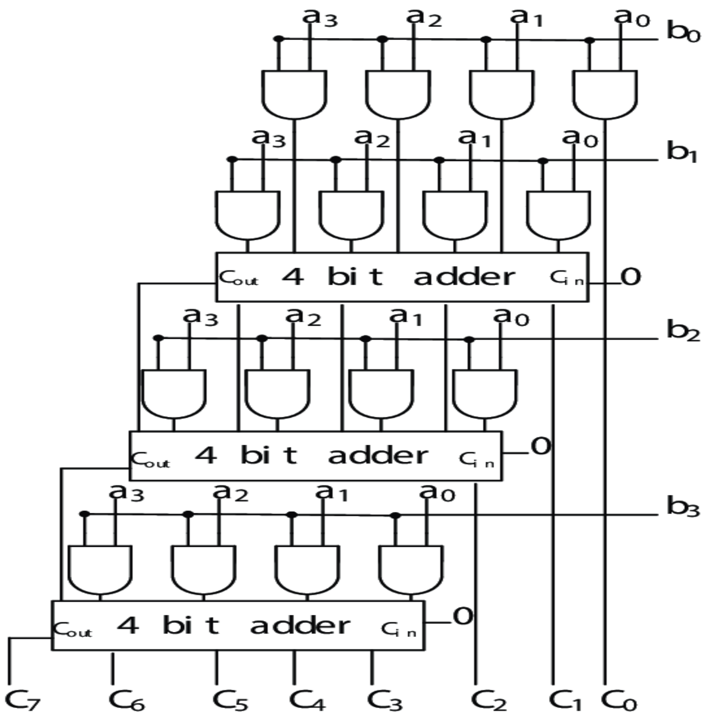



Figure 4. 4x4 Sequential Finite Field Multiplier

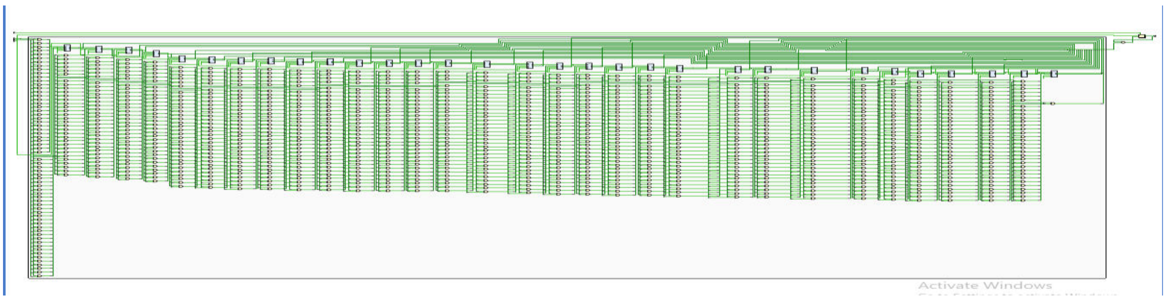


Figure 5.RTL schematic

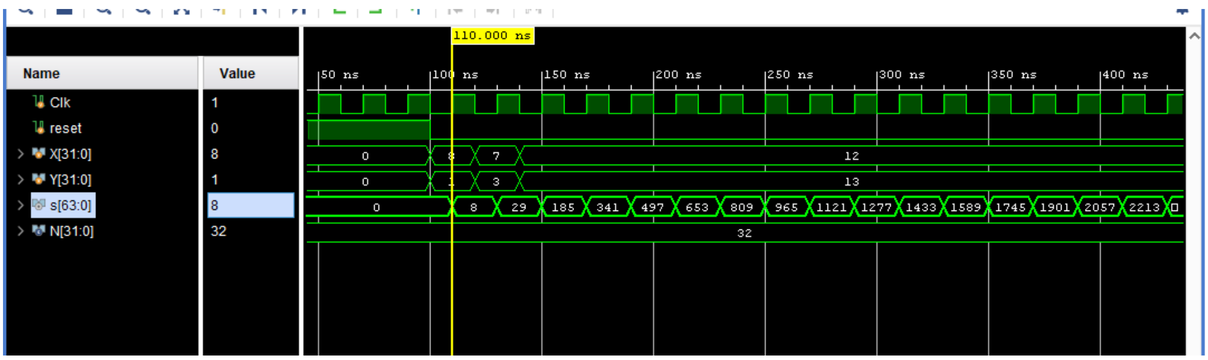
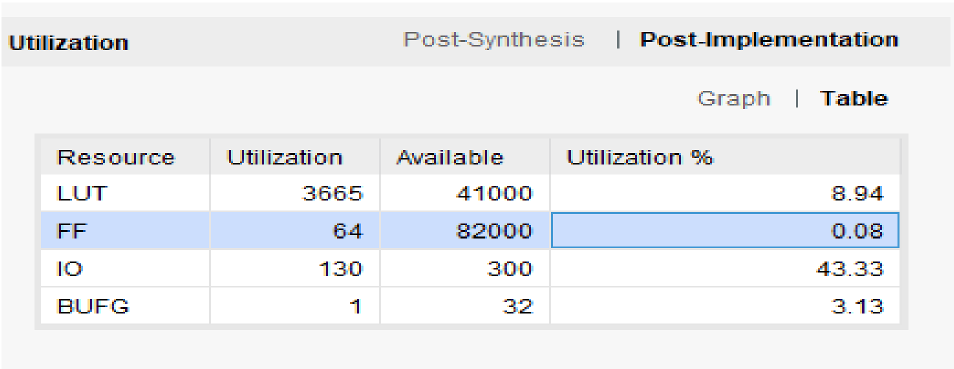


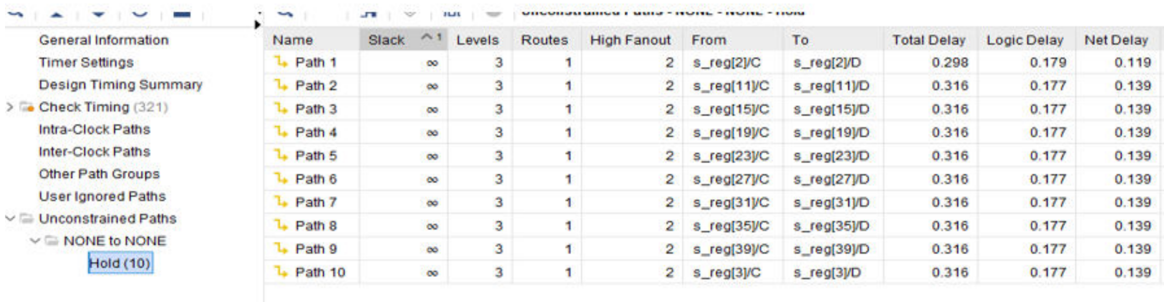

Figure 6. Simulation Output



| Resource | Utilization | Available | Utilization % |
|---|---|---|---|
| LUT | 3665 | 41000 | 8.94 |
| FF | 64 | 82000 | 0.08 |
| IO | 130 | 300 | 43.33 |
| BUFG | 1 | 32 | 3.13 |



Figure 7. Area Summary.



| Name | Slack | Levels | Routes | High Fanout | From | To | Total Delay | Logic Delay | Net Delay |
|---|---|---|---|---|---|---|---|---|---|
| Path 1 | ∞ | 3 | 1 | 2 | s_reg[2]/C | s_reg[2]/D | 0.298 | 0.179 | 0.119 |
| Path 2 | ∞ | 3 | 1 | 2 | s_reg[11]/C | s_reg[11]/D | 0.316 | 0.177 | 0.139 |
| Path 3 | ∞ | 3 | 1 | 2 | s_reg[15]/C | s_reg[15]/D | 0.316 | 0.177 | 0.139 |
| Path 4 | ∞ | 3 | 1 | 2 | s_reg[19]/C | s_reg[19]/D | 0.316 | 0.177 | 0.139 |
| Path 5 | ∞ | 3 | 1 | 2 | s_reg[23]/C | s_reg[23]/D | 0.316 | 0.177 | 0.139 |
| Path 6 | ∞ | 3 | 1 | 2 | s_reg[27]/C | s_reg[27]/D | 0.316 | 0.177 | 0.139 |
| Path 7 | ∞ | 3 | 1 | 2 | s_reg[31]/C | s_reg[31]/D | 0.316 | 0.177 | 0.139 |
| Path 8 | ∞ | 3 | 1 | 2 | s_reg[35]/C | s_reg[35]/D | 0.316 | 0.177 | 0.139 |
| Path 9 | ∞ | 3 | 1 | 2 | s_reg[39]/C | s_reg[39]/D | 0.316 | 0.177 | 0.139 |
| Path 10 | ∞ | 3 | 1 | 2 | s_reg[3]/C | s_reg[3]/D | 0.316 | 0.177 | 0.139 |



Figure 8. Delay Summary.

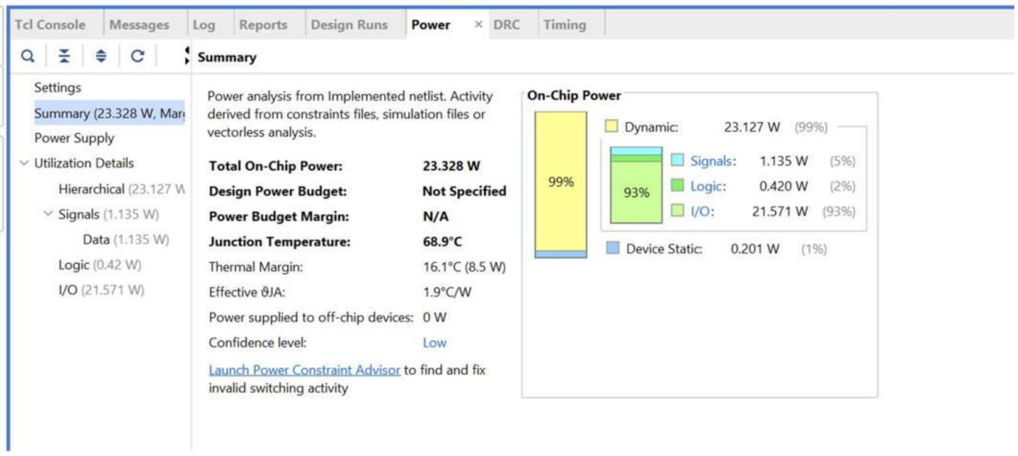



Figure 9. Power Summary.

Table 1. Comparison Table

| Parameter | Existing method | Proposed method |
|---|---|---|
| **LUTs** | 4195 | 3665 |
| **Time Delay** | 0.450ns | 0.361ns |
| **Power Consumption** | 298mw | 267mw |

## 5. CONCLUSION

Pipelined large word length digital multipliers are difficult to design under the constraints of core cycle time (for nominal voltage), pipeline depth, power and energy consumption and area.

Low level optimizations might be required to meet these constraints. In this work, we have presented a method to reduce by one the maximum height of the partial product array for 64-bit MAC has been developed. This reduction may allow more flexibility in the design of the reduction tree of the pipelined multiplier.

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