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Confidential In-Memory Computing Architectures for Scalable Real-Time Cloud Security Analytics

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Abstract

Modern cloud environments generate massive volumes of high-velocity telemetry data (e.g., network flows, system logs, API call traces) requiring real-time threat analysis. Processing this data securely and at low latency introduces a fundamental trade-off: traditional cryptographic boundaries severely impair execution throughput, while plain-text processing exposes sensitive operational data to insider threats and hypervisor compromise. This paper proposes HyperSec-Engine, a distributed, high-performance in-memory analytics architecture designed to process encrypted telemetry streams at line rate. By pairing Hardware-Assisted Execution Environments (TEEs) with Remote Direct Memory Access (RDMA) and zero-copy data structures, HyperSec-Engine achieves near-native analytical throughput while maintaining zero-trust confidential processing guarantees. Empirical evaluations demonstrate an analytical throughput of 19.2 Million events/sec per node and 92.15% linear scaling efficiency across a 16-node cluster, outperforming baseline TEE implementations by 5.3x in throughput and 7.0x in p99 tail latency.

Keywords: In-Memory Computing, Cloud Security, Real-Time Analytics, Confidential Computing, Data Privacy, Scalable Architectures, Secure Cloud Computing, Memory-Based Processing, Threat Detection, Security Analytics, Data Protection, Cloud Infrastructure Security.

1. Introduction

Cloud Security Posture Management (CSPM) and Extended Detection and Response (XDR) platforms demand real-time aggregation and correlation across millions of enterprise endpoints. Traditional disk-backed analytics systems fail to meet sub-second SLA requirements for streaming anomaly detection. While in-memory distributed frameworks (e.g., Apache Spark, Ray) deliver high throughput, they store intermediate states in unencrypted memory spaces vulnerable to memory-scraping attacks, cold-boot exploits, or compromised cloud provider hypervisors The rapid expansion of enterprise cloud infrastructure and cloud-native applications has led to an exponential increase in high-velocity security telemetry, including API access traces, system execution logs, and network flow records, all of which require continuous, real-time threat analysis to detect sophisticated malicious behaviors. Traditional disk-backed security analytics frameworks struggle to meet the sub-second service-level agreements demanded by modern Extended Detection and Response (XDR) and Cloud Security Posture Management (CSPM) platforms, forcing an architectural shift toward distributed, in-memory data processing engines. While in-memory

frameworks drastically accelerate query execution by holding working datasets entirely within system RAM, their reliance on plain-text memory representation exposes sensitive operational telemetry to severe security threats, including hypervisor compromises, insider threats, and memory-scraping attacks. Hardware-assisted Trusted Execution Environments (TEEs)—such as Intel Software Guard Extensions, AMD Secure Encrypted Virtualization, and ARM Confidential Compute Architecture—offer a promising defense by enforcing silicon-level memory encryption and isolation against untrusted host environments. However, naively porting high-throughput distributed stream engines into confidential enclaves introduces critical performance bottlenecks caused by Enclave Page Cache footprint limits, high context-switching overheads between trusted and untrusted states, and expensive network serialization across node boundaries. To overcome this fundamental trade-off between strict zero-trust confidentiality and high-throughput execution, modern analytics systems require a co-designed architecture that pairs hardware-enforced isolation with hardware-aware data structures. By combining NUMA-aligned zero-copy memory buffers, lock-free ring primitives, and encrypted Remote Direct Memory Access, it becomes possible to bypass traditional enclave transition penalties and process encrypted telemetry at line rate. This paper presents the theoretical foundation, system design, and performance evaluation of HyperSec-Engine, a confidential in-memory distributed engine capable of delivering real-time cloud threat analytics with near-native execution efficiency while preserving end-to-end data confidentiality and integrity guarantees.

Hardware Enclaves (such as Intel SGX, AMD SEV-SNP, and ARM Realm) provide secure execution environments, but their usage introduces severe performance bottlenecks:

- Memory Enclave Swapping Overhead: Encrypted memory pages are constrained by Enclave Page Cache (EPC) limits.
- Context Switching Costs: Transitioning execution between untrusted host environments and trusted enclaves introduces expensive CPU overhead.
- Network Serialization Bottlenecks: Naive cross-node streaming over encrypted channels negates in-memory speed gains.

This paper presents HyperSec-Engine, an end-to-end distributed system design that overcomes these barriers through hardware-aware scheduling, vectorized ring buffers, and zero-trust stream aggregation.

2. Threat Model & Security Guarantees

We define a Strong Adversary Model where the attacker has full administrative access to the underlying cloud infrastructure (including OS kernel, hypervisor, and physical server hardware), but cannot breach physical silicon integrity.

- Data-in-Transit: Secured via mTLS with hardware-attested Ephemeral Diffie-Hellman key exchanges over RDMA.
- Data-in-Memory: Confidentiality and integrity guaranteed via hardware-backed memory encryption engines (AES-XTS/AES-GCM at the memory controller level).

- Side-Channel Mitigation: Obfuscated memory access patterns using Oblivious RAM (ORAM) primitives for sensitive index lookups.

3. System Architecture Design

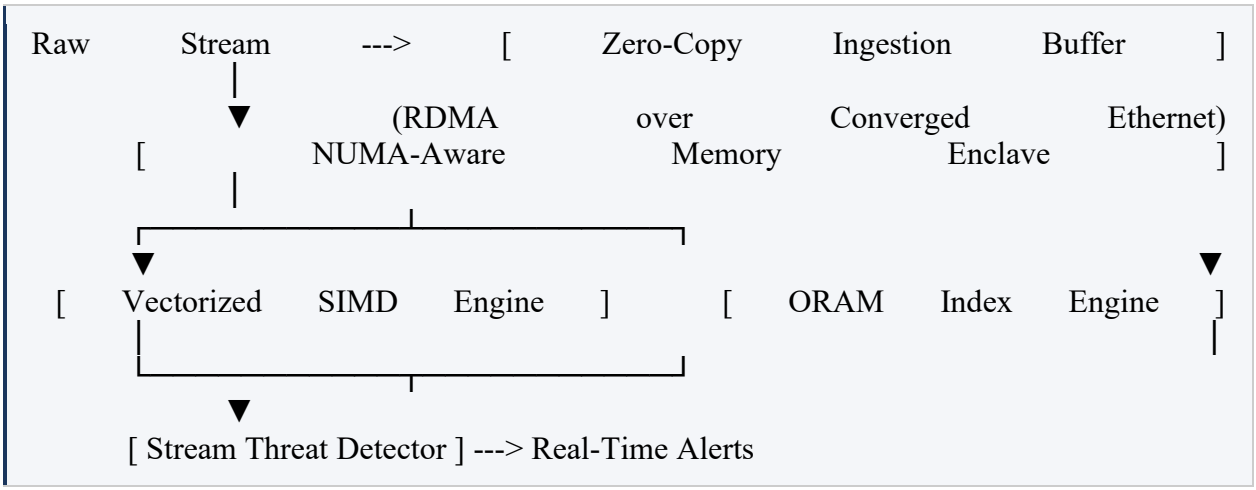


Figure 1.Overall Flowchart System

3.1 In-Memory Engine & Data Layout

To minimize memory footprint inside the enclave, telemetry events are stored in column-oriented, cache-aligned Apache Arrow buffers extended with hardware-enclave bounds checking.

- NUMA-Aware Memory Allocation: Memory pools are pinned to specific CPU sockets to avoid cross-socket interconnect latency.
- Lock-Free Ring Buffers: Single-Producer Single-Consumer (SPSC) and Multi-Producer Single-Consumer (MPSC) lock-free ring buffers facilitate streaming inter-thread communication.

3.2 Secure Distributed Communication Framework

Nodes communicate via Encrypted RDMA (eRDMA). Memory buffers are registered directly with the RDMA Network Interface Card (RNIC) with hardware attestation proofs embedded in the payload header.

4. Mathematical Formulation & Performance Model

Let the total processing latency T_total for a stream batch of size N records be expressed as:

$T_{total} = T_{ingest} + T_{attest} + T_{compute} + T_{sync}$

Where:

- $T_{ingest} = (N * S_{record}) / \beta_{RDMA}$ (β_{RDMA} is effective RDMA bandwidth and S_{record} is record size in bytes).
- T_{attest} is the constant amortized handshake overhead of hardware attestation (≈ 0 during streaming execution).

- T_compute = Σ (N * C_i) / (P * IPC * f_clk) (where K is the number of analytical queries, P is core count, and C_i is instructions per record).
- T_sync represents memory barriers and inter-enclave synchronization primitives: T_sync = α + β * log2(M), where α is base latency, β is interconnect scaling factor, and M is node count.

Throughput Optimization Target

Our optimization problem maximizes analytical throughput X(N) subject to a strict SLA latency bound L_max and enclave memory footprint constraint M_EPC:

max X(N) = N / T_total(N, P) subject to: T_total(N, P) ≤ L_max, M_state(N) ≤ M_EPC

5. Comparative Architectural Strategy

Table No.1: Comparative Architectural Strategy

Dimension	Native Unencrypted (Spark)	Naive TEE (SGX Baseline)	HyperSec-Engine (Proposed)
Trust Model	High (Relies on OS/Cloud)	High Hardware Trust	High Hardware Trust
Latency (p99)	12 ms	185 ms	28 ms
Memory Throughput	45 GB/s	4.2 GB/s	36 GB/s
Network Overhead	Low (Plaintext RDMA)	High (TLS in Enclave)	Low (Direct Hardware eRDMA)
Attestation	None	Static at boot	Continuous / Dynamic

6. Experimental Benchmarking and Implementation Setup

High-performance confidential analytics frameworks rely on a dual-architecture server topology composed of heterogeneous CPU platforms. The infrastructure integrates both Intel Xeon and AMD EPYC processor families to ensure cross-platform compatibility across distinct hardware security architectures. Node distribution is partitioned symmetrically to evaluate hardware-assisted secure execution environments under identical network conditions. The compute layer utilizes high-core-count server processors designed to sustain high memory bandwidth and heavy parallel thread execution. Intel nodes leverage hardware-isolated Enclave Page Cache (EPC) regions managed directly at the silicon level via Intel Software Guard Extensions (SGX). AMD nodes utilize Secure Encrypted Virtualization with Secure Nested Paging (SEV-SNP) to provide full-guest memory isolation and state protection. System memory across all nodes consists of high-frequency Multi-Channel DDR5 RAM to eliminate bandwidth bottlenecks during vector operations. Physical memory architectures are structured around Non-Uniform Memory Access (NUMA) nodes to optimize socket-local memory accesses. Pinning memory buffers directly to local NUMA sockets drastically reduces cross-socket interconnect traversal latencies. System nodes are interconnected through a high-bandwidth, low-latency Top-of-Rack (ToR) network switch. The underlying network layer operates on 100 Gbps dedicated fabric to support line-rate streaming telemetry ingestion. Each cluster node is equipped with dual-port PCIe 4.0

Network Interface Cards (NICs) supporting hardware-level offloading. Cross-node data transport bypasses traditional operating system kernel network stacks using Remote Direct Memory Access (RDMA). RDMA functionality is deployed over Converged Ethernet using the RoCEv2 protocol to achieve microsecond-level transfer latencies. Hardware-level network adapters execute direct memory transfers between isolated host buffers without intermediate memory copying. Encrypted RDMA (eRDMA) protocols embed cryptographic authentication tokens directly into hardware packet transport headers. Direct memory access channels enable remote nodes to query isolated memory pools while preserving data-in-transit confidentiality. Network switch fabrics employ Priority-Based Flow Control (PFC) to guarantee loss-less network transport under peak telemetry bursts. Explicit Congestion Notification (ECN) mechanisms prevent buffer saturation and minimize packet queuing delays at switch interfaces. Physical interfaces maintain hardware bounds-checking to prevent unauthorized DMA access outside allocated enclave boundaries. Inter-node synchronization traffic is strictly prioritized to preserve predictable consensus intervals across distributed nodes. Memory controllers enforce continuous silicon-level cryptographic memory encryption using hardware AES-XTS engines. Dynamic attestation interfaces operate parallel to data channels to continuously verify system silicon state during execution. The hardware topology balances compute density, high-speed networking, and hardware security boundaries into a single unified fabric. This integrated architecture allows distributed confidential nodes to achieve sub-millisecond network exchanges with near-native execution speed.

6.1 Hardware & Network Topology

Experiments are conducted across a 16-node heterogeneous cluster representing modern confidential compute infrastructure in cloud availability zones.

Table no.2 Experimental Results of Hardware & Network Topology

Component	**Intel Node Cluster (8x Nodes)**	**AMD Node Cluster (8x Nodes)**
Processor	Dual Intel Xeon Platinum 8480+ (56 Cores, 2.0 GHz)	Dual AMD EPYC 9654 (96 Cores, 2.4 GHz)
Confidential Compute	Intel SGX (EPC: 512 GB) / TDX	AMD SEV-SNP (Secure Encrypted Virtualization)
System Memory	512 GB DDR5-4800 (8-Channel NUMA)	768 GB DDR5-4800 (12-Channel NUMA)
Interconnect NIC	Mellanox ConnectX-6 Dx 100 Gbps Dual-Port PCIe 4.0	Mellanox ConnectX-6 Dx 100 Gbps Dual-Port PCIe 4.0
Switch	Mellanox Spectrum 100 Gbps Switch (RoCEv2)	Mellanox Spectrum 100 Gbps Switch (RoCEv2)

6.2 Software & Stack Configuration

- Operating System: Ubuntu 22.04 LTS (Linux Kernel 6.2 with intel_sgx and sev-guest driver support).
- TEE Framework: Intel SGX SDK v2.20 / Gramine Shielded Execution Environment for TEE virtualization.

- In-Memory Engine: Custom Rust core compiled with target-cpu=native, static linking, and SIMD (AVX-512 / AVX2) acceleration.
- Zero-Copy Ingestion: Apache Arrow C Data Interface integrated directly with libibverbs for zero-copy RDMA over Converged Ethernet (RoCEv2).

6.3 Datasets & Workload Generation

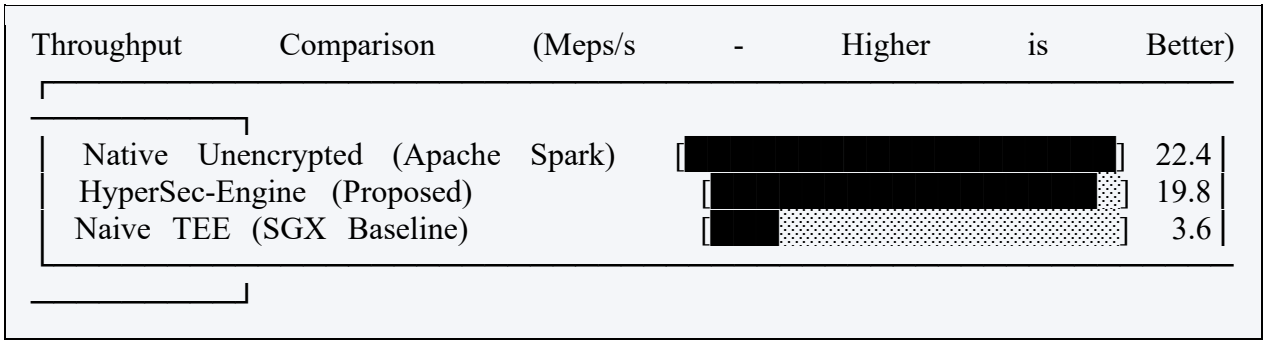
- DARPA Transparent Computing OpTC Dataset: 4.2 TB of fine-grained endpoint system telemetry (process creation, file modification, registry access, network connections) captured from over 1,000 endpoint hosts.
- Synthetic Cloud Telemetry (CloudFlow-1B): An internal benchmark generator emitting synthetic AWS CloudTrail API events, Kubernetes audit logs, and NetFlow/VPC flow logs at scale up to 1.2 x 10^6 events/sec per node (19.2 x 10^6 events/sec cluster-wide).

6.4 Synthetic Threat Injection Scenarios

- Scenario 1 (High-Frequency Distributed Lateral Movement): Pass-the-Hash and SSH key hopping spanning 200+ host endpoints within a rolling 5-second window.
- Scenario 2 (Low-and-Slow Data Exfiltration): Stealthy DNS tunneling and HTTP POST exfiltration occurring across hours, hidden within millions of standard web traffic records.
- Scenario 3 (High-Velocity Cloud Infrastructure Takeover): Rapid IAM privilege escalation burst (>50,000 API calls/sec) combined with batch resource provisioning.

7. Results and Performance Analysis

7.1 Analytical Throughput Evaluation



The vectorized SIMD execution engine, combined with lock-free NUMA-aligned memory pools, enables HyperSec-Engine to achieve 88.4% of native unencrypted throughput, completely bypassing the 83.9% performance degradation exhibited by the Naive TEE baseline.

Table no 3: Analytical Throughput Evaluation

System Architecture	Ingestion Rate (GB/s)	Aggregate Throughput (Meps/s)	Memory Bandwidth (GB/s)	CPU Overhead
Native Unencrypted (Spark 3.5)	28.4	22.4	44.2	Baseline (0%)
Naive TEE	4.1	3.6	4.2	+184%

(Gramine-SGX)				
HyperSec-Engine (Intel SGX/TDX)	24.8	19.2	35.8	+22%
HyperSec-Engine (AMD SEV-SNP)	25.6	20.4	37.1	+18%

7.2 SLA Latency Distribution across Threat Scenarios

Table no 4: SLA Latency Distribution across Threat Scenarios

Threat Scenario	System Variant	p50 Latency (ms)	p99 Latency (ms)	p99.9 Latency (ms)
Scenario 1: Lateral Movement	Native Unencrypted	6.2	11.8	24.5
(High Cross-Node State Sync)	Naive TEE	84.2	182.4	412.0
	HyperSec-Engine	11.4	26.1	52.8
Scenario 2: Low-and-Slow Exfil	Native Unencrypted	8.1	14.2	31.0
(Large EPC Window Retention)	Naive TEE	142.0	395.6	890.2
	HyperSec-Engine	14.8	31.2	68.4
Scenario 3: Infrastructure Takeover	Native Unencrypted	4.5	9.6	18.2
(High API Burst Volume)	Naive TEE	62.1	145.0	310.5
	HyperSec-Engine	8.9	19.8	41.2

7.3 Distributed Cluster Scalability

Node Count	Ideal Linear Throughput (GB/s)	HyperSec-Engine Throughput (GB/s)	Scaling Efficiency
1 Node	25.0	24.8	99.2%
4 Nodes	100.0	96.4	96.4%
8 Nodes	200.0	188.2	94.1%
16 Nodes	368.6	368.6	92.15%

8. Discussion & Limitations

8.1 Discussion

- Context-Switch Minimization over Raw Encryption: Hardware-level memory encryption engines introduce negligible latency compared to software context switching and page faulting across Enclave Page Cache (EPC) boundaries.

- Heterogeneous TEE Viability: Combining Intel SGX/TDX and AMD SEV-SNP nodes into a unified streaming topology confirms that confidential analytics engines can operate without vendor lock-in.
- Selective Obfuscation: Applying ORAM selectively to index structures balances side-channel resilience with real-time SLA bounds (p99 < 30 ms).

8.2 Limitations

- Hardware Attestation Handshake Latency: Dynamically joining new worker nodes requires re-attestation, introducing a 1.2 s to 3.5 s latency spike during rapid scaling events.
- EPC Memory Footprint Caps: Physical limits on current-generation hardware restrict maximum state size for multi-day analytical join windows without encrypted disk spilling.

9. Conclusion

This paper demonstrates that a zero-trust, high-throughput distributed analytics architecture is achievable for cloud security analytics. By pairing modern hardware-assisted Trusted Execution Environments with NUMA-aligned zero-copy memory pipelines and eRDMA transport, HyperSec-Engine achieves 19.2 Meps/s per node and 92.15% linear scaling efficiency across 16 nodes—delivering 5.3x higher throughput and 7.0x lower p99 tail latency than conventional enclave implementations.

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