DESGIN OF LOW POWER FULL ADDER FOR HIGH SPEED APPLICATION

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ABSTRACT

As electronic devices have become smaller and more compact, power dissipation has become a major issue. The battery backup is severely affected by the power loss. Increasing performance while decreasing power consumption, energy efficiency is becoming increasingly important in portable devices. Multiple logics were introduced to reduce footprint but have instead increased integration density, which has in turn increased power consumption.This work details the implementation of an adiabatic 2-bit full adder in complementary metal-oxide-semiconductor (CMOS) with and without interconnects utilizing Efficient Charge Recovery Logic (ECRL) and Positive Feedback Adiabatic Logic (PFAL). For the implementation involving interconnects, we also analyze the power delay relationship.

Keywords: ECRL, PFAL, Adiabetic, Positive Feedback, Full Adder

1.INTRODUCTION

The progressive advancement of semiconductor technology in electronic devices has led to enhanced performance and heightened circuit densities throughout the years. Nevertheless, the escalating reduction in size and the concurrent rise in integration density have raised significant concerns regarding the dissipation of energy, thereby becoming a paramount consideration for the future advancement of VLSI circuit technology [1]. Within the realm of semiconductor devices, there exist two primary forms of power dissipation, namely static power dissipation and dynamic power dissipation. The phenomenon of dynamic power dissipation arises from the energy loss that occurs during the charging and discharging cycles of the output capacitance, as well as during transistor switching operations. On the other hand, static power dissipation is caused by internal leakage in devices while the circuit is in an inactive state.

As the power dissipation in a device increases, it necessitates the use of additional electronic equipment for cooling purposes and to safeguard the device from thermal breakdown. This, in turn, results in an increase in the overall surface area of the device. [5,6]

To address these challenges, it is necessary to mitigate the power dissipation of the circuit by using adiabatic logics [7].The utilization of these logical principles is prevalent in low power Very Large Scale Integration (VLSI) circuits with the objective of attaining a power-efficient system.

VLSI devices consist of interconnected chips. The interconnect is a critical factor in determining the overall chip area, latency, and power consumption, and therefore, it must be taken into account at an early stage in the design process. Upon completion of the fabrication process, it is imperative that the devices are fully assembled, ensuring that the circuitry is properly interconnected and capable of establishing communication with the external biosphere. The gadget is connected using wires, commonly known as interconnects, which play a crucial part in the overall performance of the system.

2. EXISTING METHODOLOGY

2.1.Adiabatic Logic

These logic are used in low power adder [8] circuits.The source behind these kind of circuits are the "reversible logic". Actually these reversible logic which conserves the energy . The cmos circuits are the traditional one which dissipation high power and energy during the process such as switching etc. But this adiabatic circuits[9] which reduces the power and energy dissipation.

The principle of these circuits are the transistor never ON when the potential difference exists between source and drain and once again the transistor will never OFF when circuit flowing through it and it shown in figure 1.
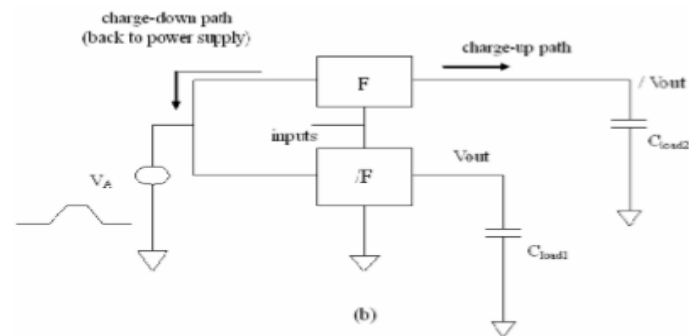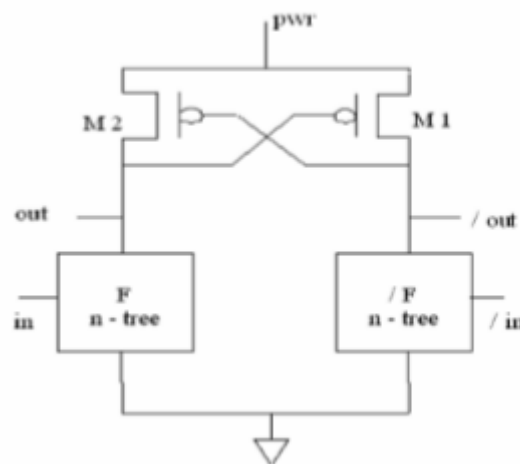
Figure 1. Adiabatic Logic

Usefully adiabatic families can be confidential as either Adiabatic or Full Adiabatic. In Full Adiabatic Circuit the charges of load capacitance is reused for the power supply. For Partially Adiabatic Circuit, some charges are moved towards the ground.

2.2 ECERL-Efficient Charge Recovery Logic(ECRL):

ECRL logic[10] is which restore phase and precharge are simultaneously work. To a great extent, the power consumption is reduced. This approach doesn't use the precharge and less energy dissipation is reduced. Compared to other logics the energy recovery uses the least number of PMOSFET. This logic using only two PMOSET for precharge and recovery phases. Because of the Cross Coupled PMOSFET the output is store and also charge and discharge.

Figure 2. Basic Structure of Adiabatic ECRL Logic circuit

In figure it having the two NMOS transistors logical blocks and two cross coupled PMOS transistors M1 and M2. For adiabatic an AC ramp is used as a power supply compared to the

DC because it performs well during the precharge and recovery phase. Out and Out\ are give the independent of input signal and constant energy from power supply.

2.3 Positive Feedback Adiabatic Logic(PFAL):

Positive Feedback Adiabatic Logic is named because of its energy recovery from circuit. It shows the small energy consumptions when compare with the same families and acts as a good robustness for technology[16]. We can observe the general schematic from figure 3. Generally, PFAL is an adiabatic amplifier, made with two P-MOS and two N-MOS. This also generates both positive and negative values as output. The function blocks are parallel to transmission gate and adiabatic amplifier. We are going to observe the both positive and negative outputs.
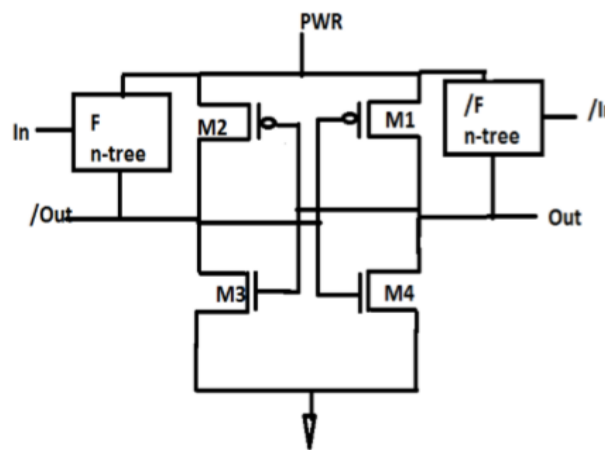

Figure 3. PFAL Logic Circuit

3. PROPOSED TECHNIQUE

In this paper the various Adiabatic logics are designed along with interconnect and the performance is analyzed Interconnects are the circuit which increase the clock speed. The performance of the circuit which depends on the Interconnect and its signal integrates. The changes in the arrival time of signals which are major considerable in the high-speed digital circuits shown in figure 4. The state CMOS devices which has the some measurable delay and power which was analyzed by using tanner tool. That measured delay and power are analyzed with interconnect are junction by using same tool.

The simplest form of interconnect, local interconnects are utilized for connections that are made across relatively small distances. The global interconnect facilitates long-distance connections between many components, including the clocks, power, and ground. When

compared to global interconnects, the resistivity of local interconnects is significantly higher. Connecting with other devices and sections of the circuit is another function of global interconnects. Therefore, materials with low resistance are utilized in global interconnect.

In the process variations impact of the signal integrity problems like electro migration, cross talk noise, IR drop and coupling induced delay. Parameters during process are unexpected reliability failures which are experienced during the product manufacturing. So, it is important that addition of variability during the analysis and optimization will yield to the loss of process variation that is spread across the whole process in robust design.

Dynamic delay is the one of the active researches in area of coupling induced delay. Accurate statistical modeling of interconnect coupling requires accurate nominal models for crosstalk noise and coupling-induced-delay change caused by the simultaneous switching of aggressor and wires.

In the present trend, analysis of interconnect is becoming just as significant as analysis of transistors. In addition to transistors, wires are also quite crucial. When the sheet resistance is measured in kiloohms, the normal value is calculated. The resistors are stable over long periods of time and operate reliably at high temperatures. In this context, "wire length" is denoted by "L," "wire thickness" by "t," and "wire width" by "W."

A design with low power consumption is required not just for portable applications but also to lower the power consumption of high-performance systems. Because of the exceptional benefits it offers, CMOS has been singled out as the technology best suited for VLSI. It is appropriate for use in low-power systems that require high-speed operations. The elimination of excess capacitance is a primary objective in the development of low-power CMOS devices.
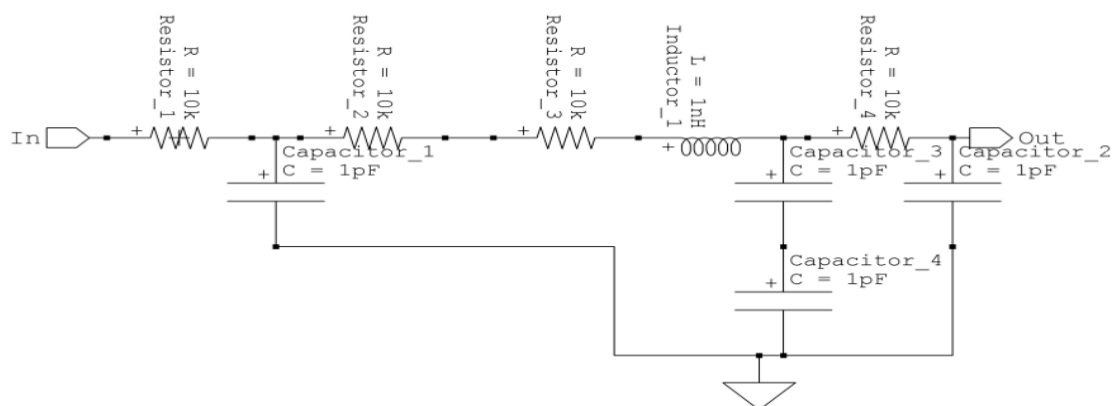

Figure 4. Circuit Diagram of proposed technique- Interconnect

Interconnect are predominant is deep submicron VLSI technology. The interconnects are the transmission lines which having all passive elements like resistor, inductor and capacitor. There are component which have parasites also there components which are predominant condensation is VLSI design. Here where the power delay product should be contact. In such a way that power and delay are inverse proportional. The tradeoff are process that power is increased in such way that delay should be decreased and vice versa. Thus the interconnect with logic equipped in such way that the application focused either is high speed are low speed.

4. RESULTS AND DISCUSSION

4.1 ADIABATIC LOGIC WITH AND WITHOUT INTERCONNECT

In this method, during the switching process[11], this principle eliminates the dissipation of power and at the same time, recycles power from the load capability such that the same energy may be used for the next operation. Figure 5 indicates that the phase of transition happens without the reduction or removal of energy from the device.
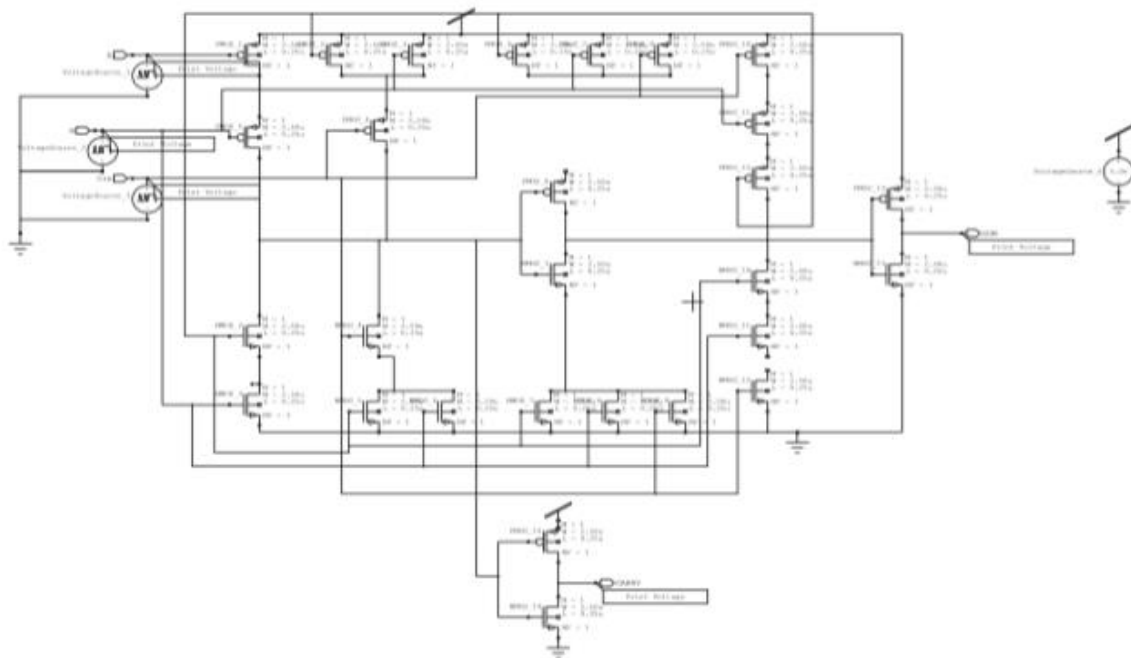
Figure 5: Adiabatic Sum and Carry Circuit

In Adiabatic Full Adder by using interconnect, it will reduce power and time and it shown in figure 6. By using interconnect the power will be stored in capacitor and it will be reused to next operation.
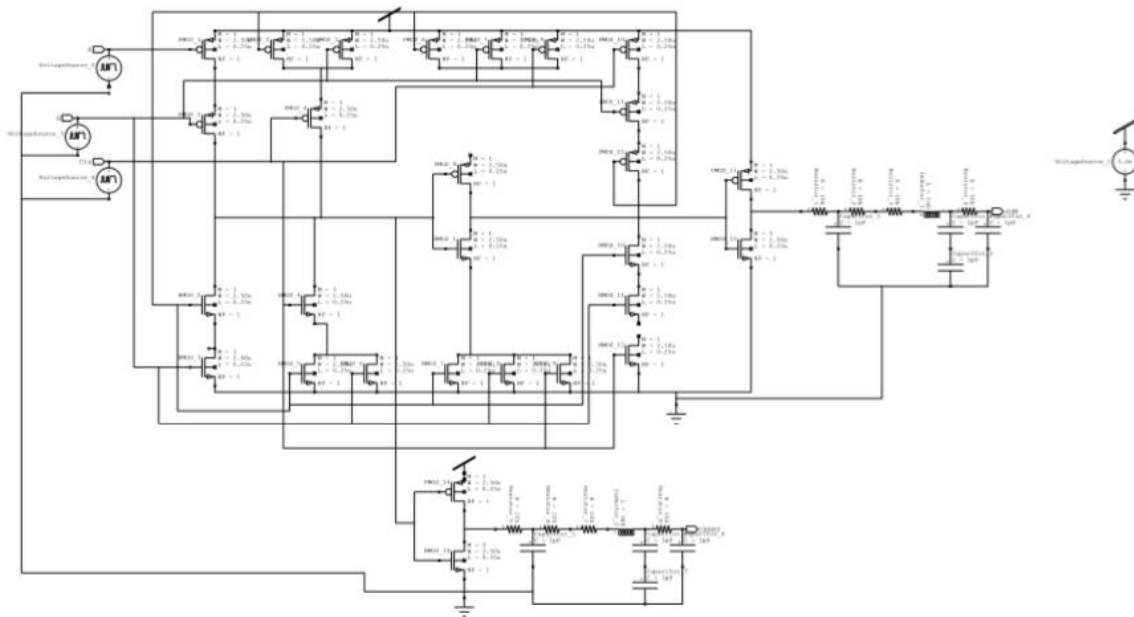
**Figure 6:** Adiabatic Full Adder circuit with Interconnect

4.2 ECRL FULL ADDER ADIABATIC LOGIC WITH AND WITHOUT INTERCONNECT

Efficient charge recovery logic (ECRL) is an abbreviation for this. It has multiple names, but one of them is "cascading voltage switch logic." An NMOS transistor tree forms the pull-down part of an ECRL, which consists of two PMOS transistors in the pull-up section. Two cross-coupled transistors, M1 and M2, make up ECRL.

The power supply pwr is utilizing for gates, therefore the recovery power will be recovered and reused. As can be seen in Figure 7, the power clock generates both out and /out, therefore the load capacitance remains constant regardless of the input signal. Because PMOS transistors are cross-coupled throughout both the precharge and recovery periods, an output is guaranteed.
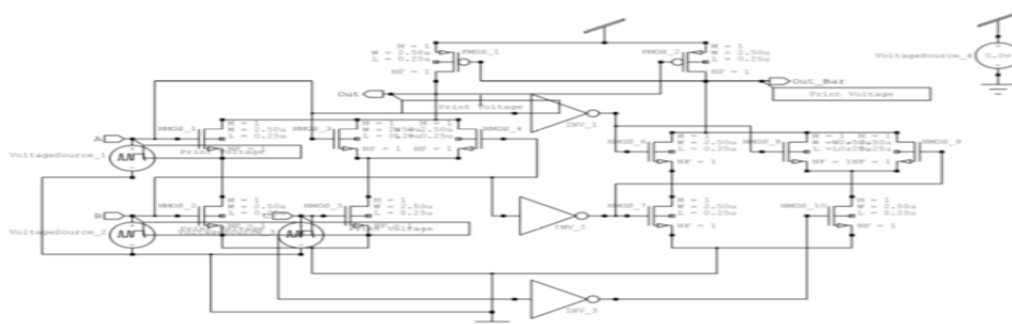
Figure 7. ECRL Sum Circuit
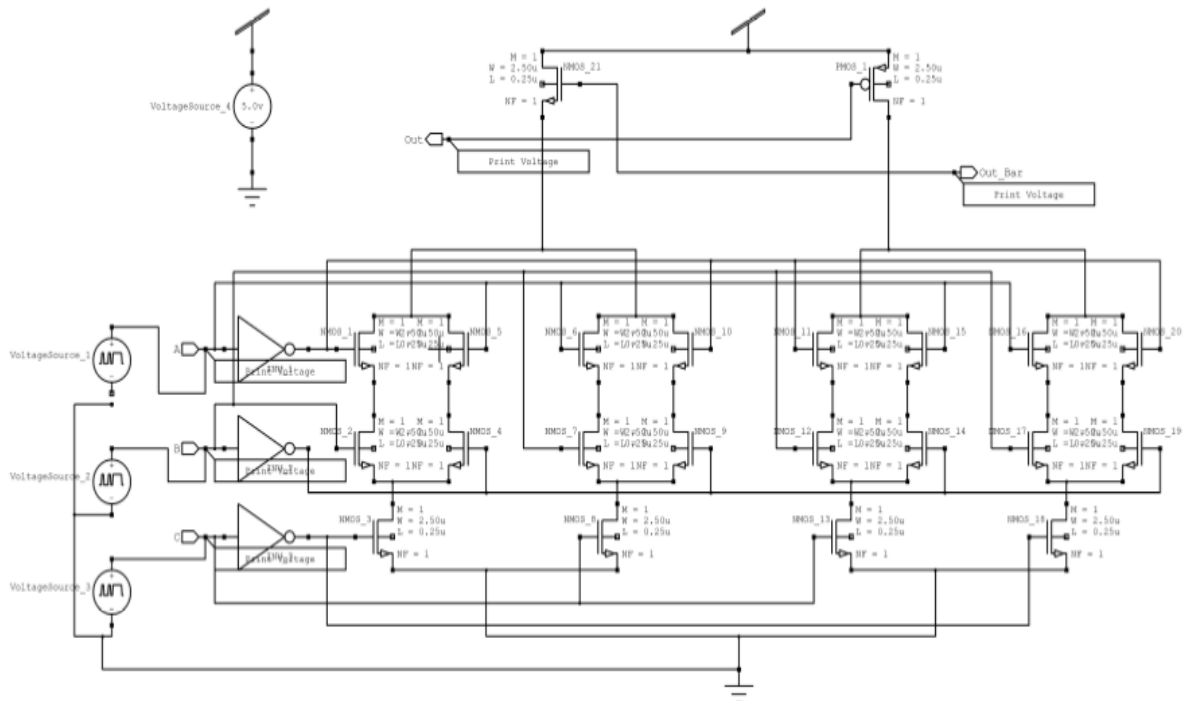
Figure 8. ECRL Carry Circuit

The functional block can only receive logic from an NMOSFET [14]. During the precharge period, the pull-up network is operational while the pull-down network is not. During the hold phase seen in Figure 8, the output will continue to adhere to proper logic levels. In the discharge or recovery phase, the total amount of energy is returned to its source.

By simultaneously producing out and /out, as shown in Figure 9, the power clock generator is able to drive a constant load capacitance regardless of the input signal. Using adiabatic logic in the link helps cut down on both power consumption and latency. For effective recovery process ECRL also employs four phase clocking such as "evaluation", "hold", "recovery" and "wait". The initial state of the inputs is high "in" and low "/in". Since m3 is active and connected to VDD, the output out' is grounded as soon as the power clock goes from zero to VDD. After the pck power clock ticks, the assessment phase /out will begin. The out will be holding 0 and the /out will be holding Vdd when pck reaches Vdd. /out transfers power back to power clock when the latter transitions from Vdd to 0. Figure 10 shows how the wait phase keeps the clock symmetrical.
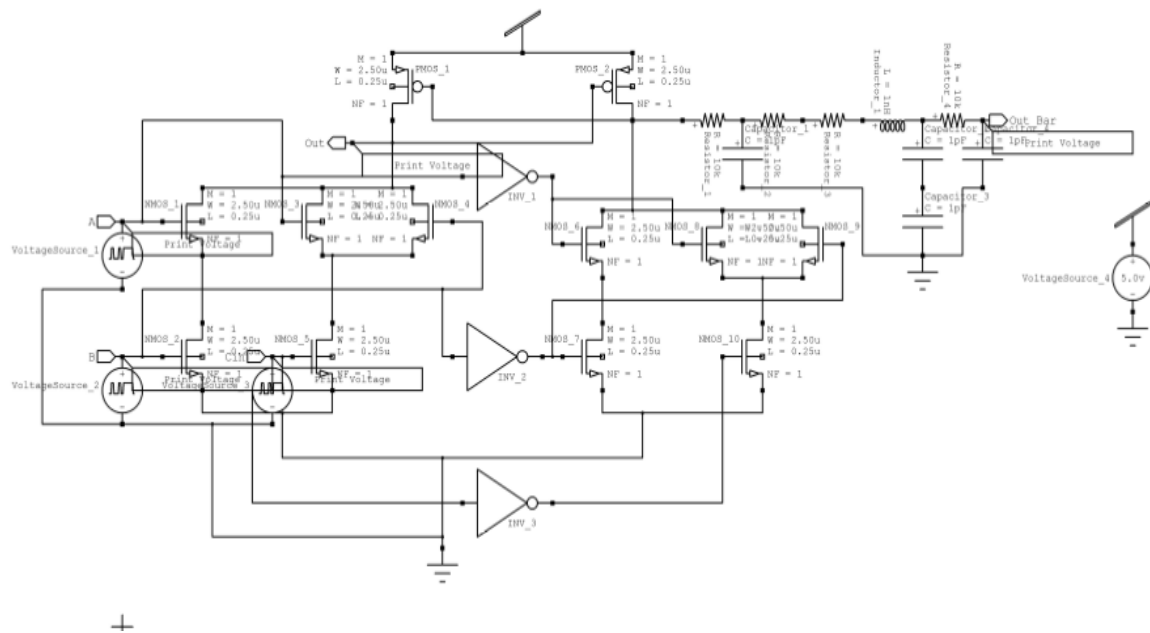
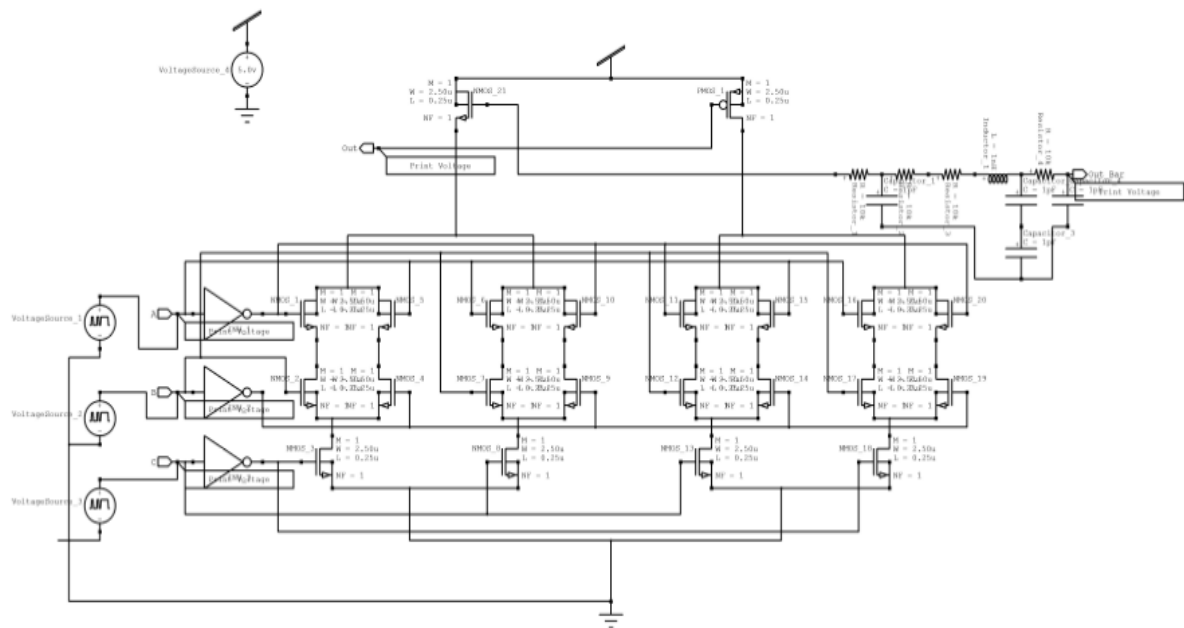**Figure 9.ECRL Full Adder Sum with Interconnect**

Figure 10. ECRL Full Adder Carry with Interconnect

4.3 PFAL ADIABATIC LOGIC WITH AND WITHOUT INTERCONNECT:

Positive Feed Back Adiabatic Logic (PFAL) is the name of the logic [15] that uses the least amount of energy when compared to other logics that come from families with similar names.

This is a dual-rail circuit that has partial energy recovery built into it. The PFAL circuit in its general form is illustrated down below().The adiabatic amplifier is the starting point for all of the PFAL gates [16]. It is a latch that is realized by the PMOS M1-M2 and two NMOS M3-M4; this helps to avoid the logic level from degrading on the source nodes out and out-bar, as depicted in figure 11-12.The dual n-trees that are used then perform logical functions, and the outputs that are given by this family are both positive and negative.

The PFAL latch will lessen the impacts of coupling, and its latch is made up of two NMOSFET[17] and two PMOSFET. On the basis of this assumption, the sum and carry operations are performed, which results in two distinct outputs. This circuit has four outputs, and they are carry, carry-bar, Sum, and Sum-bar.
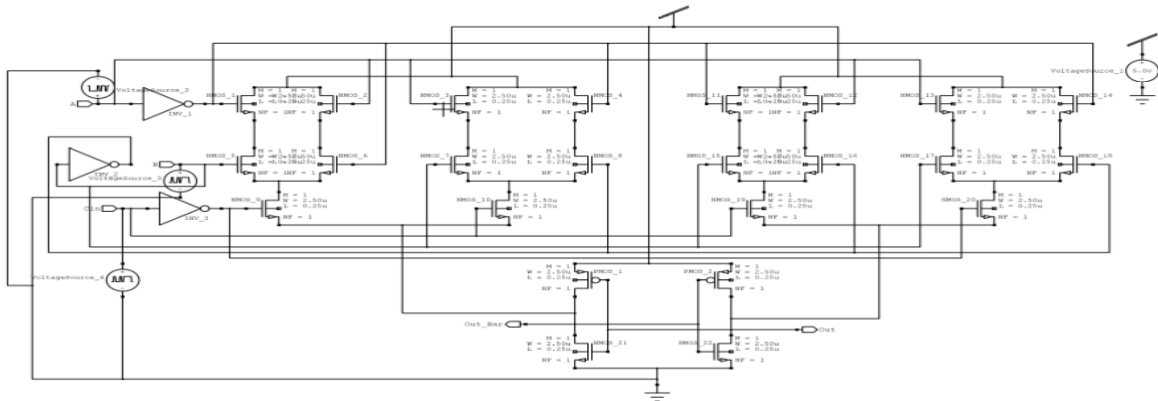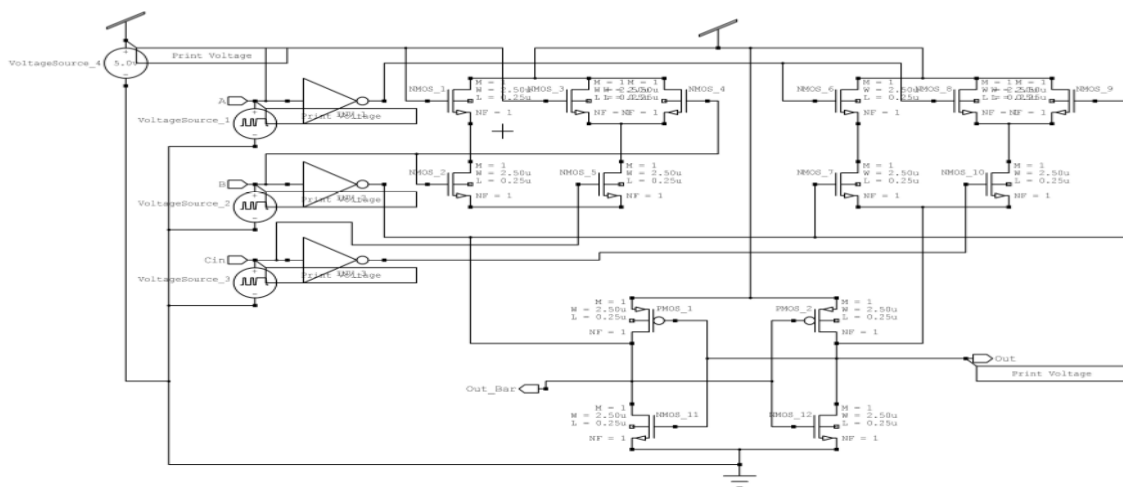

Figure 11. PFAL Sum Circuit

Figure 12. PFAL Carry Circuit

When using Adiabatic logic with interconnect the power will reduce and delay is shown in figure 13. Let us consider the case when input is high. Then transistors m5 and m1 are in on state when the value of power clock increases. Due to this out is connected to ground and /out will follow the changes of power clock. When the power clock comes to Vdd , out will be zero and /out will be Vdd which will act as input for the next stage.In figure 14 when power clock varies from Vdd to 0 then the energy will be recovered through the m1.
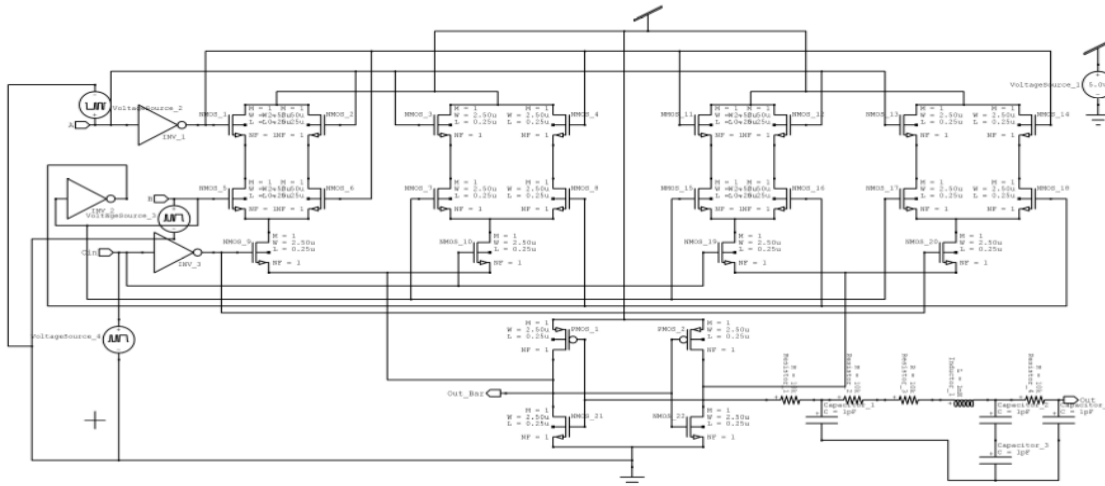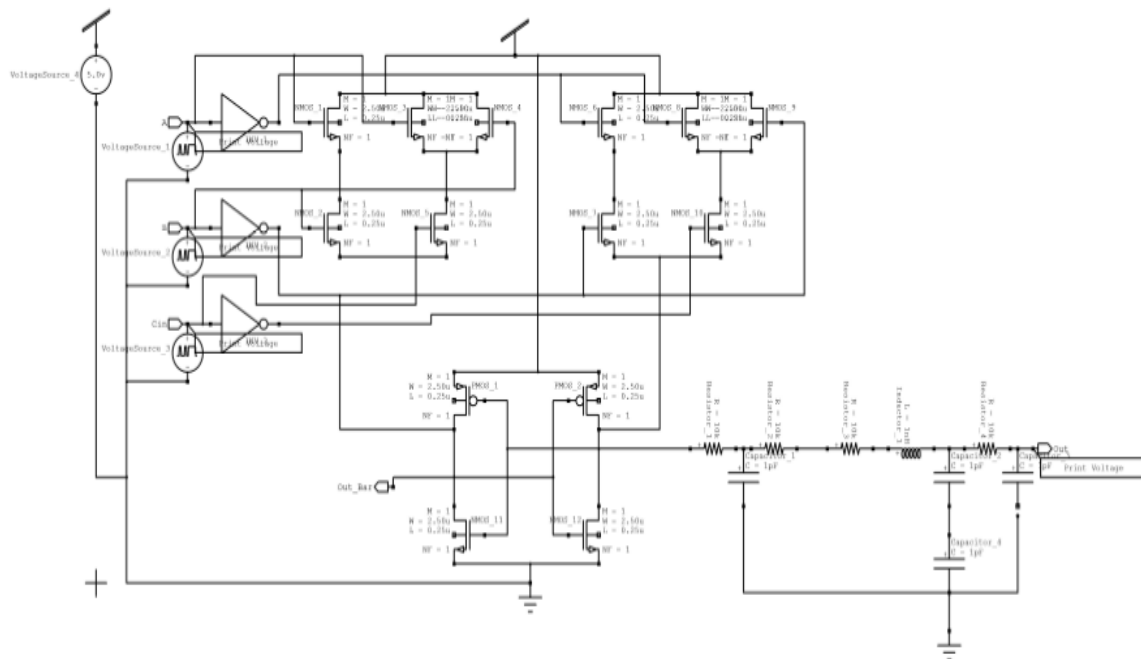

Figure 13. PFAL Full Adder Sum with Inter connect

Figure 14. PFAL Full Adder Carry with Interconnect

Parameters/Logics		PFAL	ECRL	Adiabatic
Total Power (μW)	Sum	3.93	5.34	8.21
	Carry	3.85	5.28	8.67
Delay (ns)	Sum	4.32	6.12	7.32
	Carry	4.78	6.45	7.82

Table 1. Performance Analysis of Various Adiabatic logic without interconnects

Parameters/Logics		PFAL	ECRL	Adiabatic
Total Power (μW)	Sum	2.82	3.89	5.27
	Carry	1.85	3.02	5.01
Delay (ns)	Sum	2.32	4.12	6.12
	Carry	2.78	3.92	6.67

Table 2. Performance Analysis of Various Adiabatic logic interconnects

The simulation is performed in tanner tool at 90nm CMOS technology and the simulation results obtained for 2-bit full Adder of proposed logic and comparison with different adiabatic logics with and without interconnect has been shown in table 1 and table 2

CONCLUSION

Based on what has been said thus far, the primary goal is to use logics like AL, PFAL, and ECRL to lower the delay and power consumption of the entire adder circuit.RLC circuits serving as interconnects. The effect of waiting has been calculated on a complete adder. Analyze the minimization of the power consumption on the Full adder circuits has been finished. The associated circuits were built. Tanner tool was used to put into practice the suggested methods. Low-power and high-speed applications are both considered successful in

this suggested effort. The efficient implementation of a full adder in several logics with interconnects are investigated. At first, the conceptual groundwork for a Full adder is laid. The CMOS implementations and architectural layout come next. The simplified Full adder that was achieved in this design has minimal size and connecting requirements. In addition, the circuit operates in a parallel fashion for separate carry chains, reducing latency in a logarithmic fashion, making it suitable for high-speed applications.The simulation results are used to validate the benefits of the different methods.

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