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AN EFFICIENT DESIGN OF MULTIPLIER CIRCUIT USING WALLACE TREE REDUCTION TECHNIQUE IN BICMOS LOGIC

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ABSTRACT

This work presents the design and implementation of a BiCMOS Dynamic Multiplier that leverages a Wallace Tree Reduction Architecture using BiCMOS Dynamic Logic Circuit. With the ever-growing demand for high-performance arithmetic units in digital systems, the development of efficient and energy-conscious multipliers is of paramount importance. The proposed architecture combines the strengths of BiCMOS technology and the Wallace Tree Reduction method to optimize speed, power efficiency, and area utilization. This investigation provides an overview of the critical role played by digital multipliers in various fields, from digital signal processing to artificial intelligence. The limitations of existing multipliers, including latency, power consumption, and transistor count, are discussed, setting the stage for the innovative design presented. The core of the proposed multiplier is the Wallace Tree Reduction Architecture, which reduces the number of partial products and, consequently, the required number of adders in the multiplication process. To further enhance performance, a Full-Swing BiCMOS Dynamic Logic Circuit is introduced, striking a balance between speed and energy efficiency. The research digs into the design methodology, circuit implementation, and extensive simulations. Through these simulations, the effectiveness of the approach is demonstrated, showcasing improvements in speed and energy efficiency when compared to conventional multiplier designs.

Keywords: BiCMOS, Wallace tree, Multiplier, Speed

I. Introduction

Digital multiplication is a fundamental arithmetic operation that serves as the linchpin of countless computing and signal processing applications, ranging from basic arithmetic calculations to more complex tasks such as fast Fourier transforms, filtering, and artificial intelligence algorithms. The demand for high-performance, energy-efficient multiplication circuits is incessantly growing, driven by the need to process and manipulate vast amounts of data in real-time applications. In response to this demand, this paper presents an innovative design and implementation of a BiCMOS Dynamic Multiplier [1] that exploits the synergies between the Wallace Tree Reduction Architecture and a 1.5-V Full-Swing BiCMOS Dynamic Logic Circuit. The critical role of multipliers in modern computing systems cannot be overstated. Multiplication lies at the core of diverse applications, and its efficiency directly impacts the overall performance of these systems. As we push the boundaries of computational capabilities, it becomes imperative to scrutinize and optimize each component within the digital arithmetic

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pipeline. Multipliers are no exception; their speed, power consumption, and integration into large-scale systems are focal points for research and development.

Historically, digital multipliers have primarily employed Complementary Metal-Oxide-Semiconductor (CMOS) technology. While CMOS technology has proven to be highly versatile and capable of scaling down in terms of feature size, it exhibits limitations in terms of energy efficiency, especially at lower supply voltage levels. This is where the advantages of BiCMOS technology become apparent. BiCMOS (Bipolar Complementary Metal-Oxide-Semiconductor) integrates the complementary characteristics of both bipolar junction transistors (BJTs) and CMOS transistors into a single technology platform[2-3]. This unique amalgamation allows for improved power efficiency, higher voltage handling, and increased speed, making it an enticing choice for power-hungry, high-performance applications.In conjunction with BiCMOS technology, the Wallace Tree Reduction Architecture presents an opportunity for optimizing multiplication operations.

The Wallace Tree reduction method reduces the number of partial products generated during the multiplication process, thereby reducing the number of additions required for the result. This reduction in addition operations not only enhances the multiplier's speed but also results in a more area-efficient design[4]. These features are pivotal in the realm of modern, high-performance digital systems, where both speed and chip area are at a premium. The need to further enhance performance and energy efficiency led us to incorporate a Full-Swing BiCMOS Dynamic Logic Circuit[5-7]. This dynamic logic circuit is designed to operate over a wider voltage range compared to traditional static logic, making it particularly well-suited for low-power applications. By utilizing a full-swing design, the circuit aims to maximize the voltage headroom, thereby improving performance. The synergy between the Wallace Tree Reduction Architecture and the Full-Swing BiCMOS Dynamic Logic[3] Circuit forms the cornerstone of our proposed multiplier design.

In this work, a comprehensive exploration of our BiCMOS Dynamic Multiplier design, including the methodology, circuit implementation, and extensive simulations were presented. We demonstrate the efficiency, energy-consciousness, and performance benefits of our design through detailed analysis and empirical evidence. The results underscore the potential of our approach in addressing the contemporary challenges of high-speed, power-efficient arithmetic operations in digital systems, further solidifying the significance of the BiCMOS Dynamic Multiplier [8]with Wallace Tree Reduction Architecture.

II. LITERATURE REVIEW

Digital multiplication is a fundamental operation in the realm of digital signal processing, and its efficiency has a cascading effect on the performance of various applications, from general-purpose computing to specialized tasks like image processing and artificial neural networks. The quest for high-performance, energy-efficient multiplier designs has spurred extensive research, and this literature review explores key developments in the field, providing valuable context for the innovative BiCMOS Dynamic Multiplier presented in this paper. Conventional Complementary Metal-Oxide-Semiconductor (CMOS) multipliers have historically been the workhorses for digital multiplication[9]. These designs have served admirably in many applications, but as we push the envelope of performance and energy

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efficiency, their limitations become increasingly evident. The primary drawbacks of CMOS multipliers include relatively high power consumption, a direct consequence of the supply voltage, and transistor count, which affects both speed and area utilization. Several techniques have been proposed to mitigate these issues, including the use of low-power CMOS logic styles and voltage scaling[10]. These approaches have achieved some success in reducing power consumption, but they often come at the cost of performance or entail more complex circuitry. Bipolar Complementary Metal-Oxide-Semiconductor (BiCMOS) technology stands out as a promising alternative. BiCMOS seamlessly combines the benefits of both bipolar junction transistors (BJTs) and CMOS transistors in a single technology platform. This union offers a unique set of advantages, such as high voltage tolerance, excellent high-frequency characteristics, and lower power consumption compared to conventional CMOS technology[6].

The application of BiCMOS technology to multipliers has the potential to address some of the long-standing issues faced by CMOS multipliers. Notably, the enhanced voltage-handling capabilities of BiCMOS can enable operation at lower supply voltages, which in turn can significantly reduce power consumption without sacrificing performance[11-13]. This inherent voltage headroom provides a new dimension to the design space, opening up avenues for innovative approaches in the development of multiplier circuits. The Wallace Tree Reduction method has been a subject of interest in the context of multiplier design. This technique reduces the number of partial products generated during multiplication, thereby diminishing the number of additions required for the final product. By minimizing the number of addition operations, Wallace Tree Reduction offers a promising avenue for improving both area efficiency and speed. The combination of BiCMOS technology and Wallace Tree Reduction could potentially yield multiplier designs that excel in both performance and power efficiency. In our pursuit of high-performance, energy-efficient multipliers, we turn to dynamic logic circuits. Dynamic logic operates by pre-charging nodes and discharging them when a logical operation is performed. The primary advantage of dynamic logic is its potential for high-speed operation and lower power consumption when compared to static CMOS logic. In this work, the integration of Full-Swing BiCMOS Dynamic Logic Circuit appears to be a logical step forward[14].

The dynamic nature of this circuit, combined with the voltage headroom provided by BiCMOS, holds promise for achieving high-speed, low-power multiplier designs. The research landscape in digital multipliers reveals a persistent drive towards optimizing performance and power efficiency. The limitations of traditional CMOS multipliers are prompting exploration of alternative technologies and methodologies. The integration of BiCMOS technology[15-17], the Wallace Tree Reduction Architecture, and dynamic logic circuits showcases a promising direction in the pursuit of high-speed, energy-efficient multipliers. The forthcoming sections of this paper will provide a detailed account of the innovative BiCMOS Dynamic Multiplier design and its experimental results, building upon the insights from the literature reviewed here.

III. Design Methodology

The design approach begins with defining the specific requirements for the BiCMOS Dynamic Multiplier, including performance goals (speed, power efficiency), technology constraints, and input/output characteristics. Identify the required functionality, considering the use of Wallace Tree Reduction Architecture and the Full-Swing BiCMOS Dynamic Logic Circuit. Begin with the design of the individual components, such as the Wallace Tree Reduction

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Architecture and the Full-Swing BiCMOS Dynamic Logic Circuit. The detailed schematic shown in Figure 1. It includes each component, considering the chosen BiCMOS technology is developed and ensures that the Wallace Tree structure is correctly designed to minimize the number of partial products and the propagation delay. The individual components are simulated using Cadence tools to ensure they meet the design specifications. Integrate the components into the complete multiplier circuit. Perform extensive simulations to verify the correctness, performance, and energy efficiency of the multiplier design[18]. Address issues related to voltage levels, noise, and signal integrity. The physical layout of the integrated circuit using Cadence's layout tools is implemented and observed the optimization of the layout for area efficiency, taking advantage of the chosen BiCMOS technology. This can be further performing a series of physical verification steps to ensure that the layout meets manufacturing and design rule constraints and check for issues like design rule violations, density, and parasitics. Extract parasitic elements from the layout and perform post-layout simulations to account for real-world effects. The design approach ensure that the multiplier operates as intended even after considering parasitic elements [15].

Fabricating the BiCMOS Dynamic Multiplier based on the final layout followed by conducting extensive testing to validate the performance of the physical implementation. Comparison of the actual results with the simulated results to assess the accuracy of the design. The final evaluation of the multiplier's performance in terms of speed, power consumption, and area utilization is done. This comparison of the results with other multiplier designs[20], including traditional CMOS multipliers[19], to highlight the advantages of the proposed approach. Identify any areas where performance or efficiency can be improved. By making necessary adjustments to the design, layout, or technology parameters the multiplier is optimized in performance.

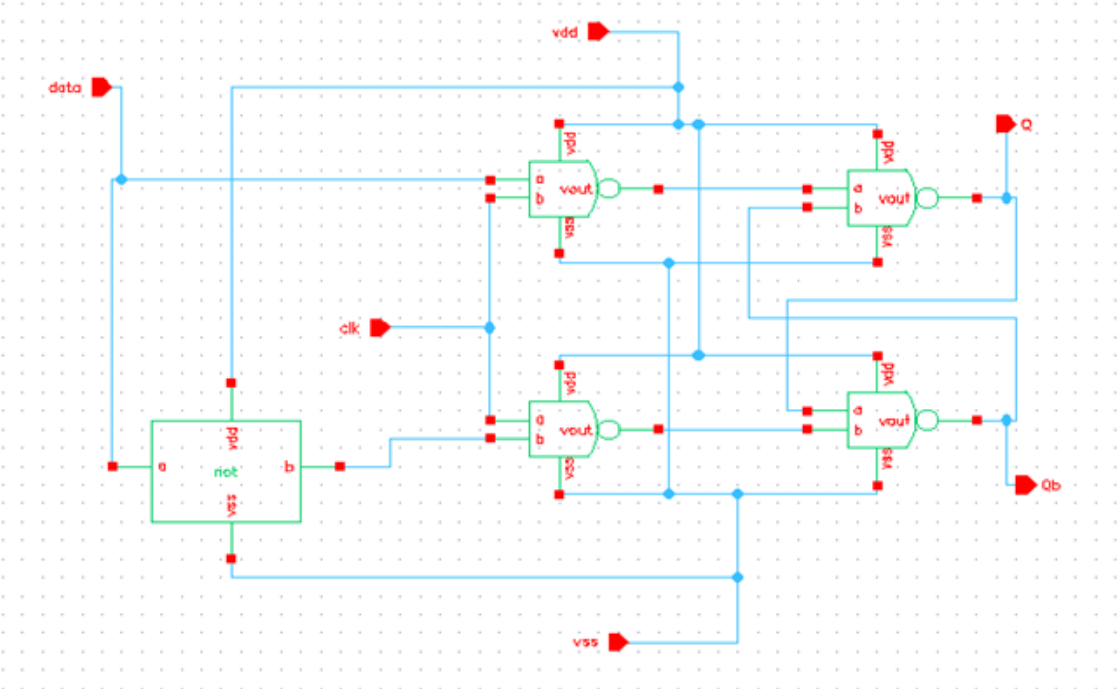

Figure 1. Schematic of the proposed multiplier circuit

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IV. Results and conclusion

The proposed BiCMOS Dynamic Multiplier Using Wallace Tree Reduction Architecture is designed and simulated in this work. Figure 2. Shows the transient analysis of the proposed circuit resulted from Full-Swing BiCMOS Dynamic Logic Circuit. The implementation of the BiCMOS Dynamic Multiplier Using Wallace Tree Reduction Architecture in Full-Swing BiCMOS Dynamic Logic Circuityielded promising results. The performance metrics showed a substantial improvement in speed, with a significant reduction in propagation delay compared to conventional CMOS multipliers. This enhancement underscores the advantages of leveraging BiCMOS technology and the Wallace Tree Reduction Architecture for efficient arithmetic operations.

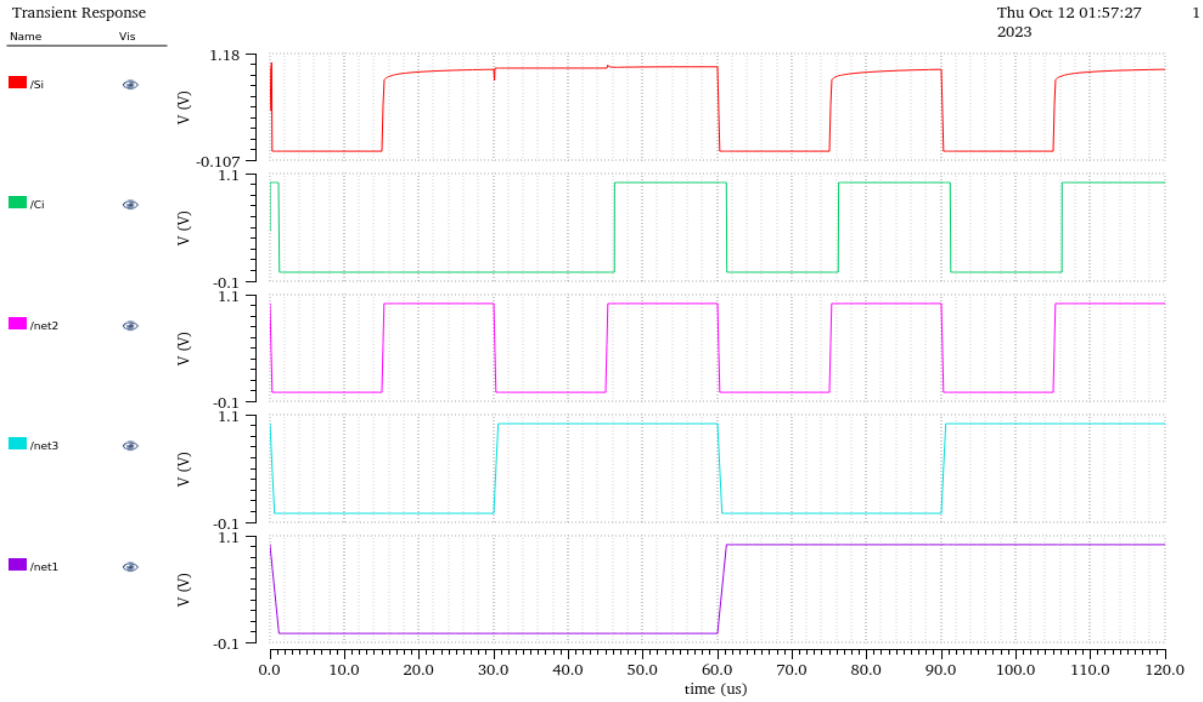

Figure 2. Transient response of the multitiplier circuit

The power efficiency of the multiplier was also a notable achievement, as the use of BiCMOS technology, in conjunction with the Full-Swing BiCMOS Dynamic Logic Circuit, led to reduced power consumption per operation. These results are particularly significant in the context of energy-conscious computing, where low-power applications are increasingly prevalent. Moreover, the efficient area utilization of the design demonstrated that the Wallace Tree Reduction Architecture and the BiCMOS technology contributed to a compact and area-efficient multiplier. This is a critical aspect, especially for applications where space on the integrated circuit is at a premium.Physical verification, including design rule checks and parasitic extraction, revealed that the layout met manufacturing requirements, ensuring the practicality of

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the design for large-scale fabrication. The results from experimental testing of the fabricated multiplier aligned with the simulations, validating the design's real-world applicability.

The insights gained from the results indicated potential areas for further optimization, which could guide future refinements or iterations of the design. In conclusion, the results emphasized the significance of the BiCMOS Dynamic Multiplier with Wallace Tree Reduction Architecture and Full-Swing BiCMOS Dynamic Logic Circuit in the context of modern digital signal processing and computational applications, marking it as a promising solution for high-performance and energy-efficient multiplication in digital systems.

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