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Design and Implementation of an Adiabatic Logic based ComputationSubsystem with Extremely Low Power Consumption

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Abstract:

The quantity of power squandered by VLSI circuits has been a serious issue in recent years. The Adiabatic logic approach is emerging as a solution to the power dissipation issue. The word 'Adiabatic' alludes to a condition change which happens without energy being lost or gained. This adiabatic switching approach significantly minimizes the amount of energy lost during switching occurrences. However, adiabatic circuits are very dependent on fluctuations in the power clock as well as parameter values. The low-power adiabatic logic based ECRL circuit works largely in the sub threshold domain and consumes less power than a CMOS version. The article explores and develops ECRL-based sub-threshold induced adiabatic circuitry on a 6:3 counter component. Tanner had been used to execute the suggested design, and the simulated results for the 45 nm cmos technology are shown.

Keywords: ECRL, subthreshold , Adiabatic

1. INTRODUCTION

The semiconductor sector has grown tremendously over the past several decades as a result of IC technology. We've gone a long way since 1958's single transistor period, with ULSI enabling the production of over 50 million transistors on a wafer. Due to the rising usage of wearable electronics, leakage current has become a critical design characteristic in contemporary electronics. Portable gadgets that run on batteries have restricted energy supply and hence a limited lifetime due to the high energy consumption. Historically, power consumption has not been a major worry owing to the accessibility of large packaging and cooling mechanisms capable of dispersing produced heat. Nevertheless, if the density & complexity of the semiconductors in the system continue to increase, it may become difficult to provide enough cooling, resulting in a

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considerable cost increase for the system. It's why we want circuitry that really is capable of minimizing power dissipation even when a large number of features are integrated onto a single chip. Our goal is to minimise the amount of energy dissipated by CMOS Technology VLSI circuits. The need for CMOS technology is mostly due to the low power dissipation as well as high integration capabilities. Nevertheless, the latest development toward ultra-low power consumption has prompted researchers to examine strategies for recovering or recycling energy from circuits. Recently, researchers have been primarily focused in determining the lower limit for energy consumption. Numerous techniques are employed to reduce energy dissipation in electronic systems, but since the majority of energy is wasted, an adiabatic methodology is the best choice for designing power as well as energy efficient systems. The quantity of energy recycled is determined by the manufacturing process, switching events, & voltage variation. [1,2,3]The article is divided into 5 pieces. Section II provides an overview of adiabatic logic. Section 3 discusses digital logic design. Section IV contains the simulation waveforms as well as adescription of the power comparison chart. and part V is devoted to concluding.

2. ADIABATIC LOGIC

The word "Adiabatic" is often used to suggest that no energy is transferred to the environment, implying that no power is dispersed. Due to the existence of dissipative components like as resistance in real-world computing, a perfect procedure cannot be attained. Nevertheless, minimal energy consumption may be accomplished by decreasing the operating speed and switching the transistors only when particular criteria are met. Adiabatic circuits seem to be energy-efficient circuits that require reversible logic' to function properly [3,4]. Adiabatic Logic in Action Adiabatic provides a method for reusing the energy held in the load capacitor, instead of discharge it to ground and waste it. The functioning of adiabatic logic circuits has been governed by many fundamental laws, including the following: never switch on a transistor while a voltage potential exists between the source and the drain, but never abruptly alter the voltage across any transistors [5,6]. Because it employs reversible logic to save energy, adiabatic logic is often referred to as ENERGY RECOVERY CMOS logic.

Families of adiabatic logic may be categorized as follows:-

Adiabatic:- In partly adiabatic , certain charge is transmitted to the ground, therefore dissipating some heat. As a result, only a portion of the energy is recovered, although these circuitry are

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simpler to design than completely adiabatic logic circuits. A component of this logic is Efficient Charge Recovery Logic (ECRL).

Fully Adiabatic:- In fully adiabatic circuits, the charge on the load capacitance are collected and sent back to the power source through the capacitances. As a result, completely adiabatic circuits are more complicated and slower than partial adiabatic circuits [7].

3. Implementation

EFFICIENT CHARGE RECOVERY LOGIC (ECRL)

ECRL introduces a novel approach that simultaneously conducts precharge as well as evaluation, hence eliminating the need for a pre - charge diode thus dissipating less energy than the previous system. circuits that are adiabatic. It is composed of a cross-coupled PMOS transistor as well as two NMOS transistors in an N-functional block that is produced using 2 cross-coupled transistor M1 & M2. A Full Swing Output is produced both in pre-charge & recovery stages due to the action of crosscouple Pmos. It utilises a four control clock and operates in the Evaluate, Hold, Recovery, and Wait modes. The clock recovers the chargegiven by the source clock effectively. Each step of the clock would be preceded by a 90° phase difference. Thus, while the preceding phase would be in the hold phase, every subsequent stage must be assessed using the logic values established during the precharge and assessment processes.

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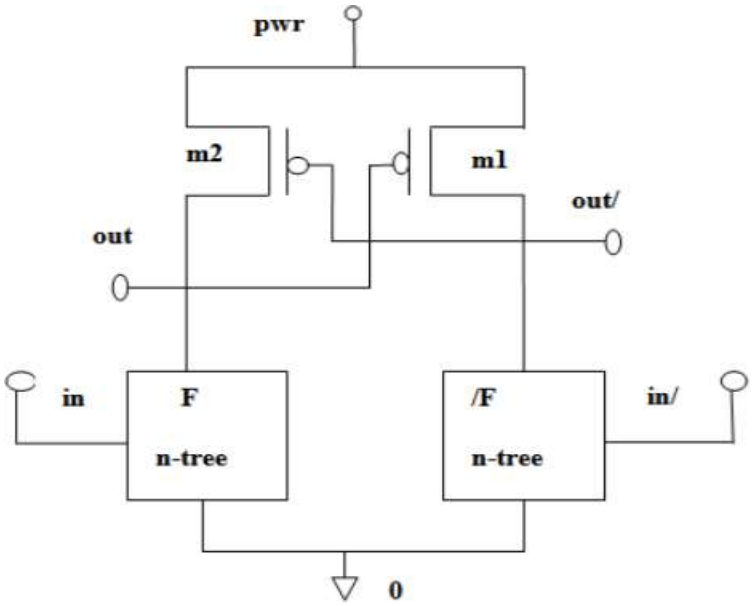
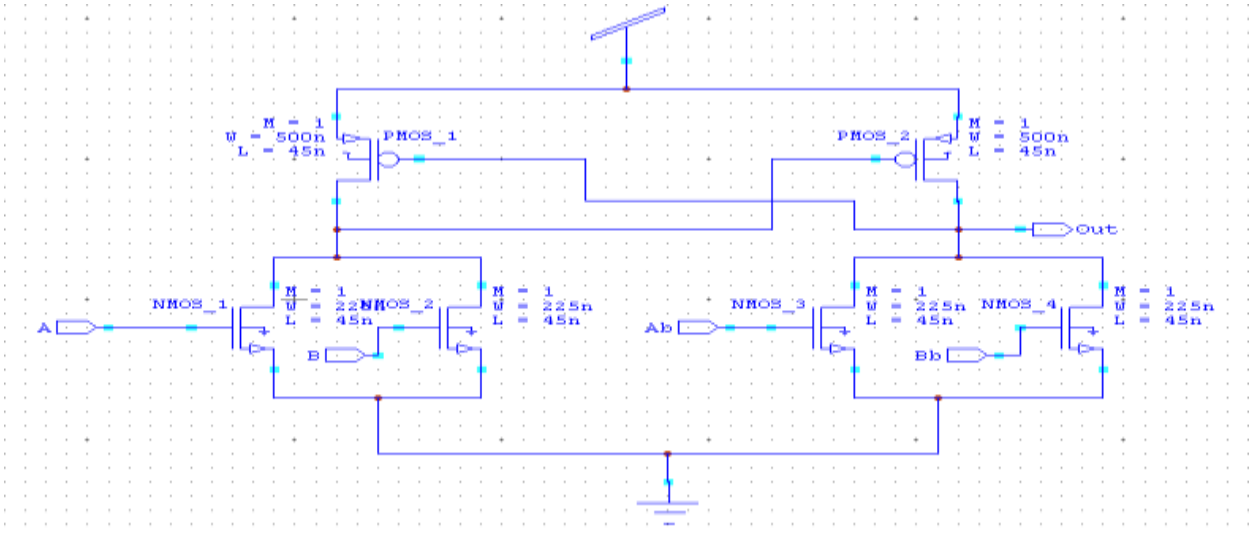


Figure 1: ECRL

ECRL would be a widely utilized adiabatic logic technology that provides complementary outputs as well as simplifies design. As previously stated, the symmetric stacking-based 6:3 compression circuit uses full adder (FA) as well as half adder (HA) modules, and therefore is developed utilising ECRL-assisted low energy adiabatic logic.



Adiabatic logic based ECRL implementation of logic gates:

Figure 2: Adiabatic logic based ECRL implementation of AND gate

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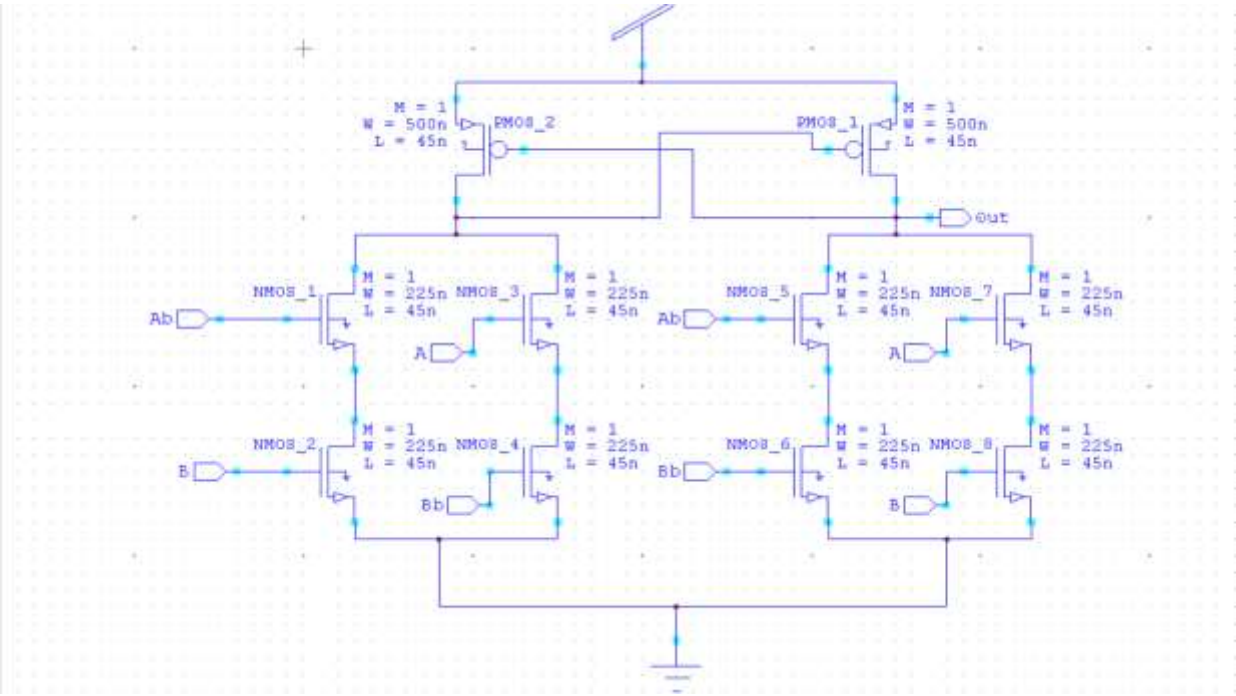

Figure 3: Adiabatic logic based ECRL implementation of XOR gate

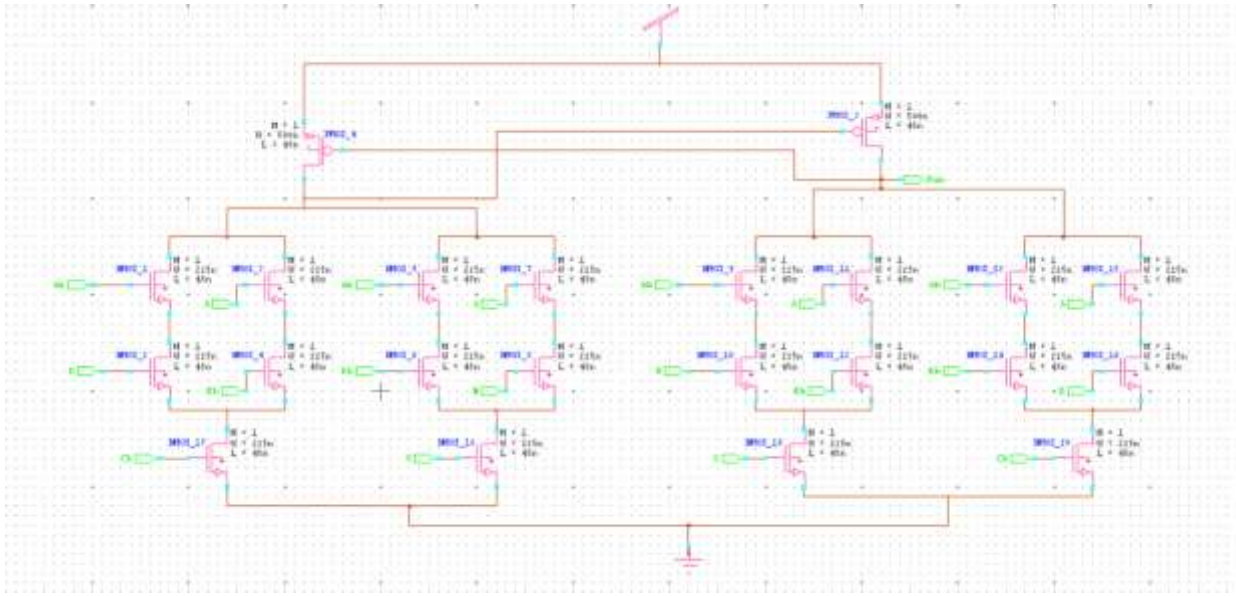

Figure 4: Adiabatic logic based ECRL implementation of Full adder Sum

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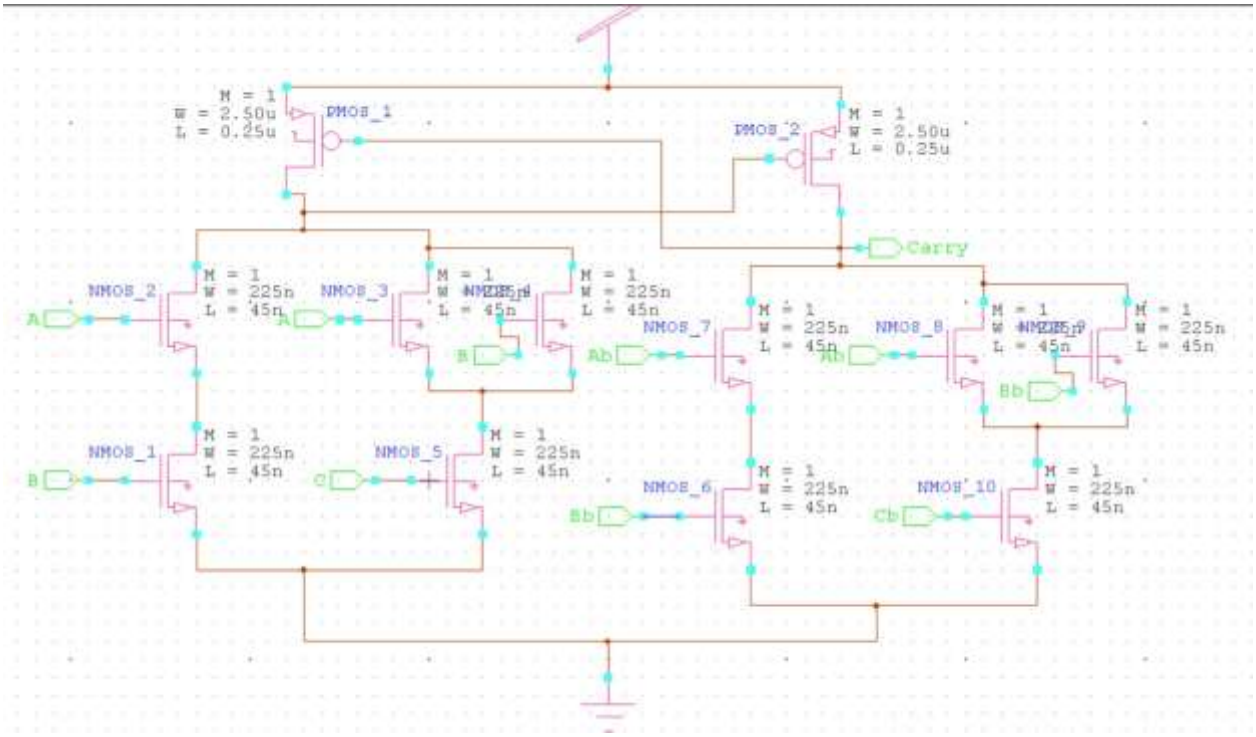

Figure 5: Adiabatic logic based ECRL implementation of Full adder Carry

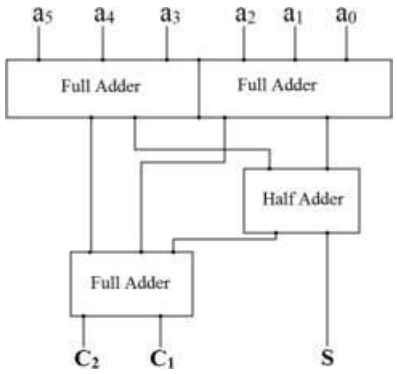

Figure 5. Schematic diagram showing conventional adder based 6:3 counter

Compressor circuits for 6:3 PPR are often designed using a mix of full adders (FA) and half adders (HA), asseen in Figure 5.

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As seen in Figure 6, the counter is implemented using ECRL-based half adders as well as full adders.

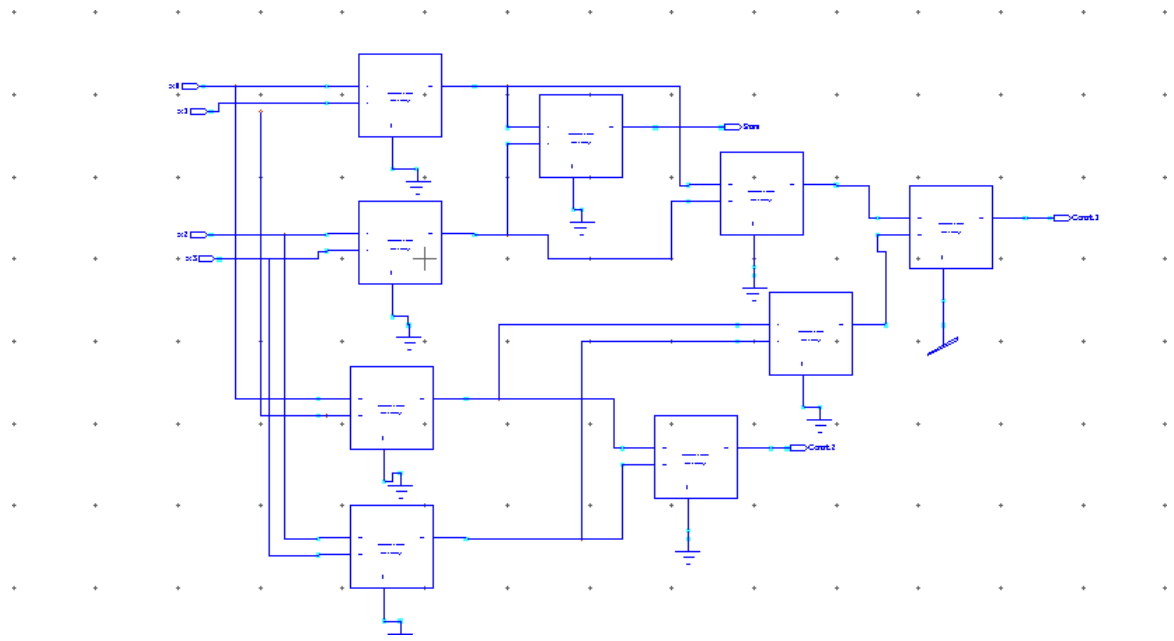

Figure 6. Schematic diagram showing ECRL based 6:3 counter

4. Simulation Results

With the suggested compressor, a 6:3 compressor circuitry including fundamental adder circuits mostly in form of ECRL-aided extreme low power adiabatic logic were developed and modelled in Tanner using 45 nm technological files.

The transient outcomes of the AND, XOR, and full adder circuits based on ECRL are illustrated in figures 7,8, 9, and 10.

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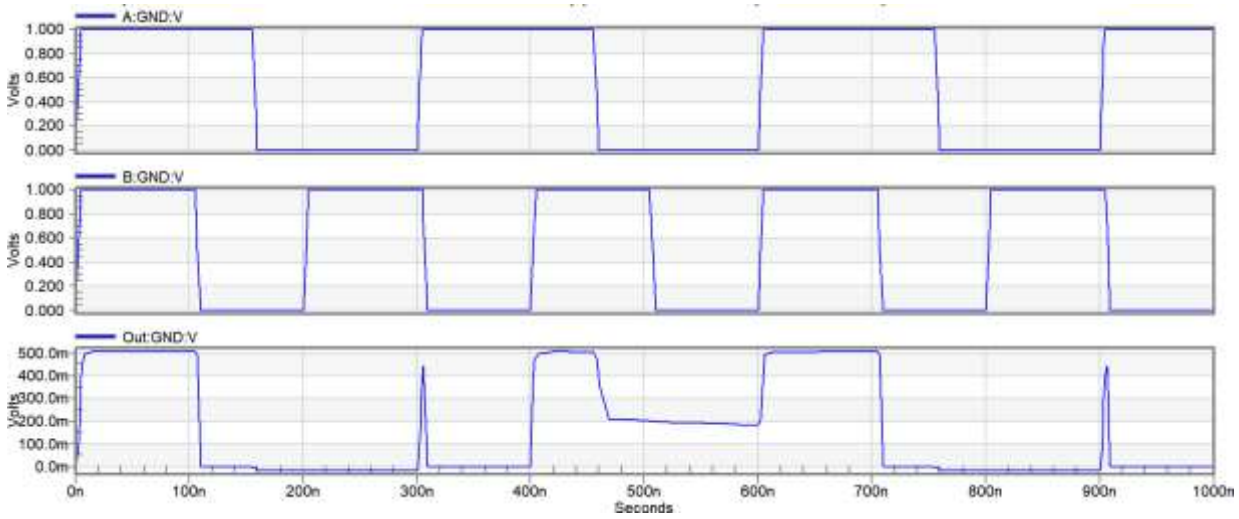

Figure 7: Transient Simulation result of ECRL based AND gate

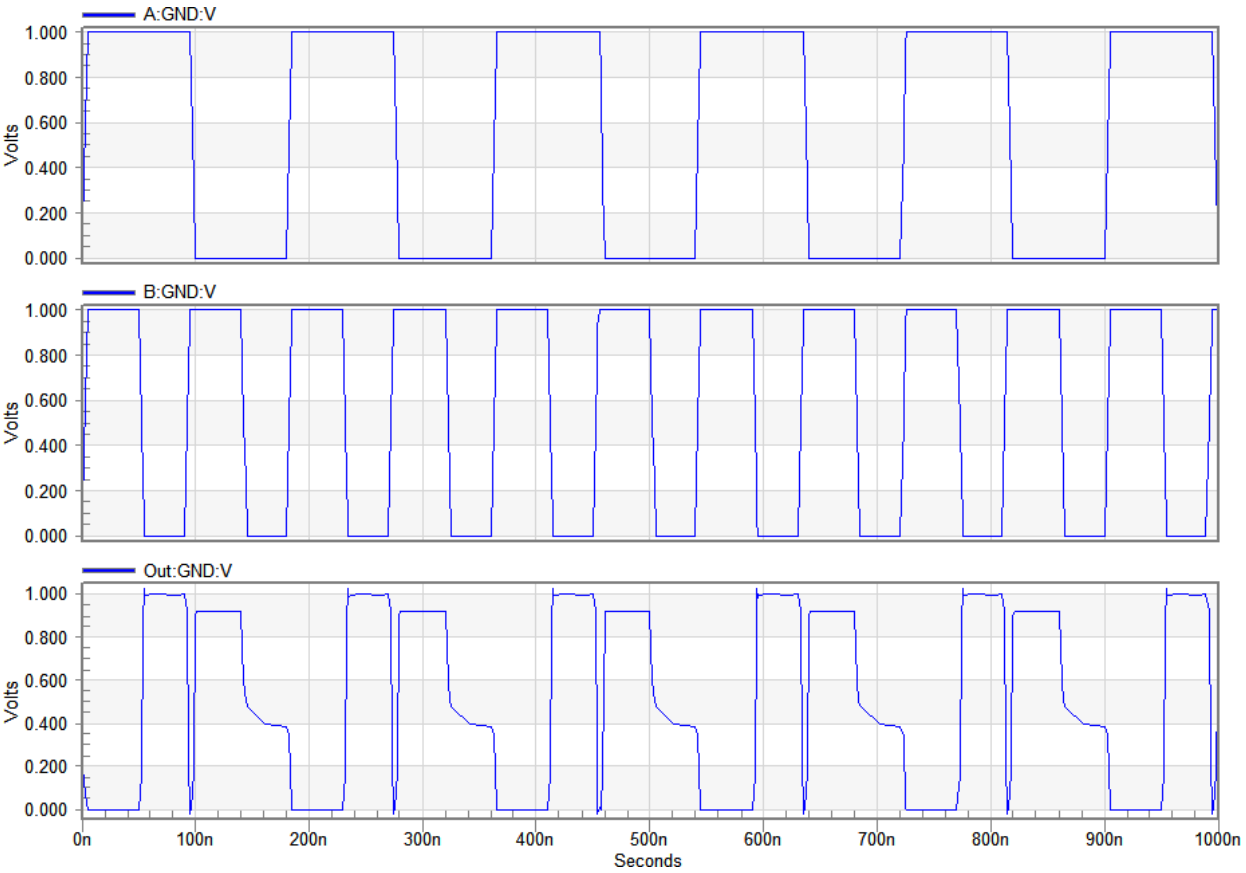

Figure 8: Transient Simulation result of ECRL based XOR gate

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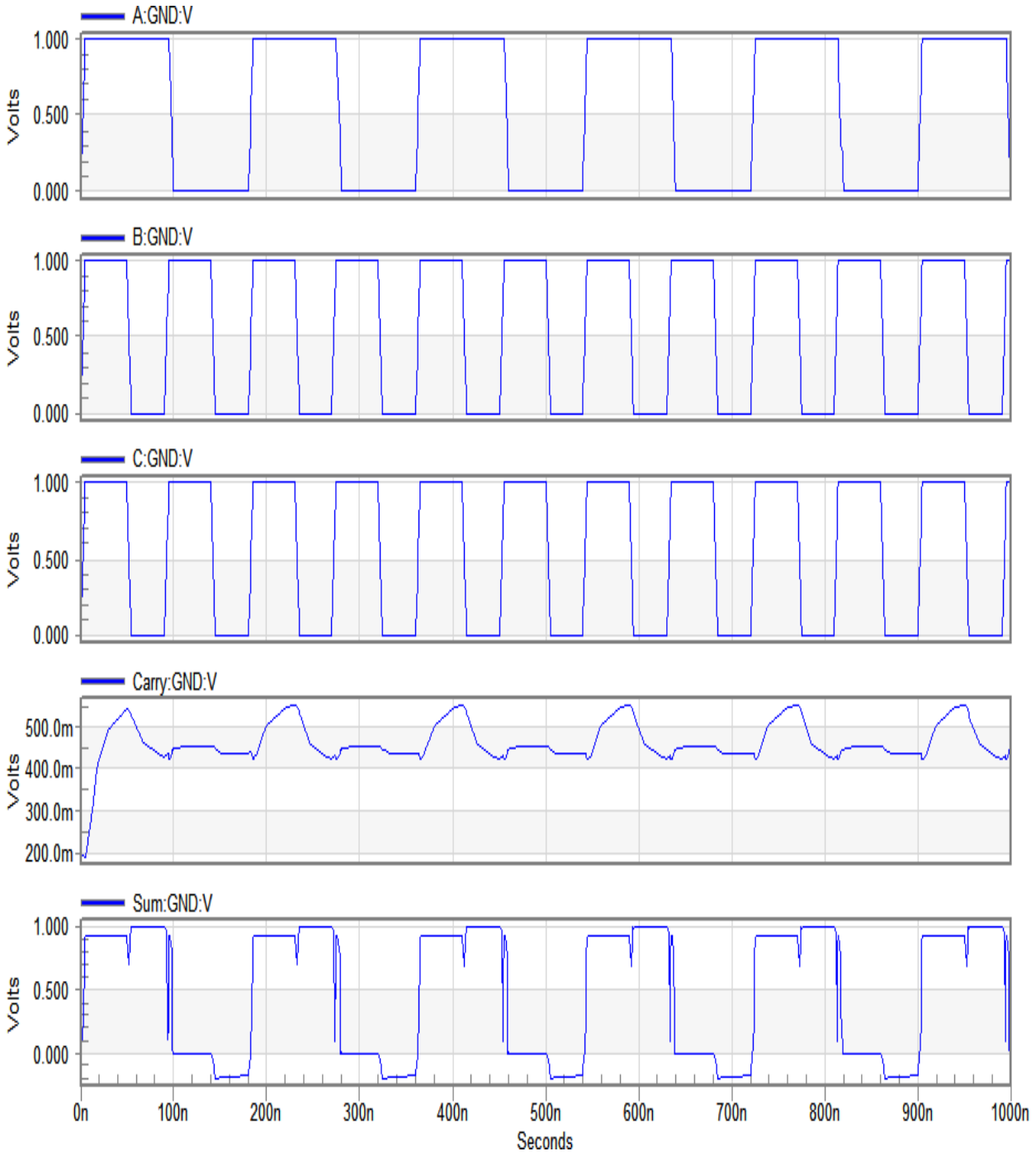

Figure 9: Transient Simulation result of ECRL based FA

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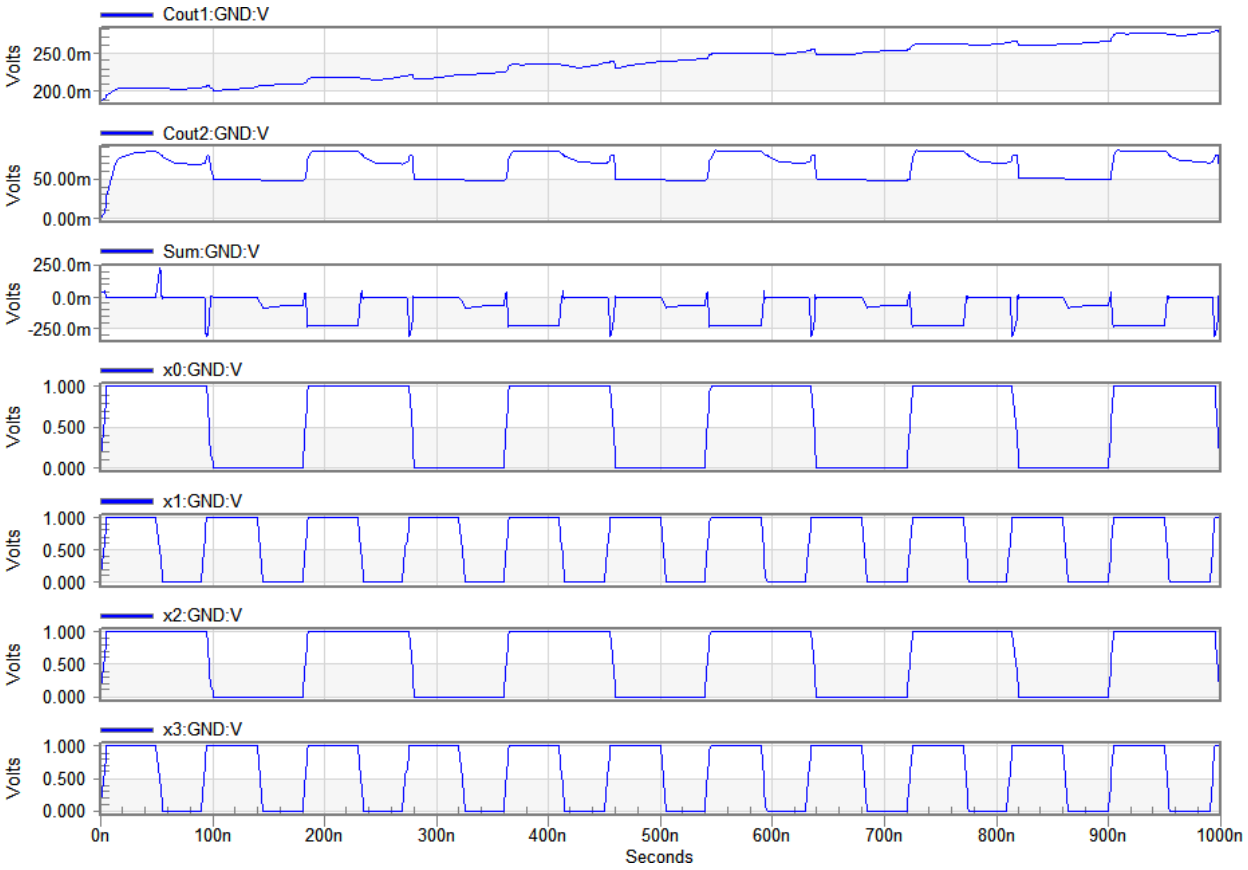

Figure 10: Transient Simulation result of ECRL based counter

The table 1 shows the power consumption of conventional and proposed counter circuits.

Design type	Average Power
Conventional	2.9239e-008 watts
Proposed	2.589e-008 watts

From the table 1, it is evident that proposed counter dissipates less power when compared with conventional counter circuit.

5. Conclusion

This article compares ECRL versus CMOS logic. We examined ECRL-modified adiabatic circuitry operatingin the sub-threshold region for an ultra-low energy 6:3 compression. Furthermore, we

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infer that ECRL circuits use less energy than traditional CMOS circuits. We also noticed that energy dissipation is reduced. Adiabatic ECRL logic consumes much less power and so performs better than traditional CMOS logic.

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