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A Novel Delay & Quantum Cost Efficient Reversible Realization of (2^i x j) Random Access Memory

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ABSTRACT:

As the conventional irreversible logic dissipates power for losing bits of information, computing engines has to be designed that do not require energy dissipation but only if computation is done logically reversible. Hence, research on reversible logic has been extensively increased now-a-days for its application in Quantum Computing, nanotechnology; QCA and Low power VLSI etc. In this paper, we have realized a Quantum Cost efficient Reversible RAM (RRAM) with a new 3x3 Reversible Gate named Modified Fredkin (MF). While approaching for RRAM we have also proposed a reversible D Flip-flop with minimum quantum cost (Qc), a write enabled reversible master slave D Flip-flop & a (i*2^i) reversible decoder which has outperformed the existing designs in terms of quantum cost, ancilla & garbage outputs. We also have analyzed the architectures in terms of logical depth (worst case delay), hardly addressed in available literature.

Keywords: Reversible Logic; Quantum Cost; Reversible D-FF; Reversible Decoder; RRAM.

INTRODUCTION:

Energy dissipation in modem processors is becoming a primary concern for the designer's day-by-day. Processors with a few billions of transistors and tens of watts are common place, limiting their use in portable devices and making heat removal in complex dense structures difficult. Hence, an increasing market for portable applications and dense complex systems will continue to encourage low power design. From the past few years due to its ability to reduce the heat dissipation Reversible logic gates are attracted by the researcher with a great attention towards it. According to the Rolf Landauer'[1-3] s principle given in 1961, the conventional logic gates or irreversible logic gates dissipates KTln2 joules of energy for the loss of I-bit information where K is the Boltzmann constant and T is the absolute temperature at which operation is performed. In irreversible logic computation, the amount of energy dissipate is directly proportional to the number of bits erased during computation. According to second law of thermodynamics, information once lost cannot be recovered by any methods.

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Internal architecture of RAM can be viewed as a 2-D array of memory cells. Each memory cell can store a single bit in a particular time. The RRAM is made up of a proposed reversible D-FF and proposed reversible decoder. Moreover, with the help of some lemmas the efficiency of RRAM has also been proved in this paper.

A reversible memory cell, i.e., [4-6] reversible sequential circuit was first designed by Fredkin and Toffoli in 1982 in which design of JK latch was introduced. Later, in 1996, Picton neither introduced the design of clock less SR-Itch using two cross-coupled NOR gate, where NOR gates were designed from Fredkin gate. In 2005, Thapliyal et.al. Introduced for the first time all the reversible latches such as D-Latch, T-Latch etc. along with their flip-flop and master-slave configuration. In 2006, Rice introduced a SR-latch without fan-out problem available in the design by Picton and subsequently designed other latches from SR. In 2007,

Thapliyal and Vinod[7-9] proposed a better design of reversible flip-flops than by Rice in terms of number of reversible gates being used and garbage outputs. In 2008, a more detailed analysis of SR-Latch is presented by Rice. A better design of all reversible latches (except SR-Latch) along with their flip-flops than that of Thapliyal (2005) and Rice (2006)[10-14] were presented by Chuang and Wang. Morita (2008) gave a discussion on how a universal reversible computer could be constructed from reversible logic elements and reversible sequential machines, but no actual hardware design was presented. This gave a direction of making RAM as it is the fundamental storage for computer system. In 2009, Hafiz [15] presented a novel design of reversible FPGA. In 2011, Morrison [16] designed a static and dynamic RAM arrays with reversible logic. Most of the previous works focused on optimization of number of gates and garbage output in the design, but in this work our goal is to optimize the proposed RRAM design in terms of three important parameters:

- Quantum Cost,
- Delay and
- Garbage output.

Basics Terms Used

A. Reversible logic gate: It is not apart advice us to dispose the results against the inputs but also advise us to incompatibly balance the inputs from the results.

B. Garbage output: It is also associate to the representation of results which are not used in the synthesis of provided activity. In assertive covering these incline compulsory to accomplish reversibility.

Constant input value}+ Input value = Garbage value + Output value

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C. Quantum cost: The quantum cost of the design is less figure of 2*2 integrated gates to exhibit the design observance the results constant.[5]It is accredit to the cost of the design in the details of the part of a primary gate.

D. Flexibility: Its indicate the collectivity of a reversible logic gates which accomplishing many activities.

E. Gate Level: This associate the fraction of objectives in the design which is useful to conceive the provided connection.

LITERATURE SURVEY:

In 1961, R.LANDAUER [1] it is argued that computing machines inevitably involve devices which perform logical functions that do not have a single-valued inverse. This logical irreversibility is associated with physical irreversibility and requires a minimal heat generation, per machine cycle, typically of the order of kT for each irreversible function. This dissipation serves the purpose of standardizing signals and making them independent of their exact logical history. Two simple, but representative, models of bistable devices is subjected to a more detailed analysis of switching kinetics to yield the relationship between speed and energy dissipation, and to estimate the effects of errors induced by thermal fluctuations.

The search for faster and more compact computing circuits leads directly to the question: What are the ultimate physical limitations on the progress in this direction? In practice the limitations are likely to be set by the need for access to each logical element. At this time, however, it is still hard to understand what physical requirements this puts on the degrees of freedom which bear information. The existence of storage medium as compact as the genetic one indicates that one can go very far in the direction of compactness, at least if we are prepared to make sacrifices in the way of speed and random access. Without considering the question of access, however, we can show, or at least very strongly suggest, that information processing is inevitably accompanied by a certain minimum amount of heat generation. In a general way this is not surprising. Computing, like all processes proceeding at a finite rate, must involve some dissipation.

In 1973, C.H.BENNETT The usual general-purpose computing automaton (e.g.. a Turing machine) is logically irreversible- its transition function lacks a single-valued inverse. Here it is shown that such machines may he made logically reversible at every step, while retainillg their simplicity and their ability to do general computations. This result is of great physical interest because it makes plausible the existence of thermodynamically reversible computers which could perform useful computations at useful speed while dissipating considerably less than kT of energy per logical step. In the first stage of its computation the logically reversible automaton parallels the corresponding irreversible automaton, except that it saves all intermediate results, thereby avoiding the irreversible operation of erasure. The second stage consists of printing out the desired output. The third stage then reversibly disposes of all the

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undesired intermediate results by retracing the steps of the first stage in backward order (a process which is only possible because the first stage has been carried out reversibly), there by restoring the machine (except for the now-written output tape) to its original condition. The final machine configuration thus contains the desired output and a reconstructed copy of the input, but no other undesired data. The foregoing results are demonstrated explicitly using a type of three-tape Turing machine. The biosynthesis of messenger RNA is discussed as a physical example of reversible computation.

In 2008, Majid Mohammdi et.al presented that quantum gates to implement the binary reversible logic gates. Quantum gates V and V+ to be represented in truth table forms. Author proved that several reversible circuit benchmarks are optimized and compare with existing work. A new behavioral model to represent the V and V+ quantum gates based on their properties. This model used to simulate the quantum realization of reversible circuits.

In 2010, D.Michael Miller and Zahra Sasanian presented the reducing the number of quantum gate cost of reversible circuits. To reduce the quantum cost improves the efficiency of the circuit. To determine a quantum circuit is to first synthesis circuits composed of binary reversible gates then map that circuit to an equivalent quantum gate realization.

In 2011, Prashant.R.Yelekar et.al described that reversible logic gates ability to reduce the power dissipation which is main requirement in VLSI design. Reversible computing which is requires high energy efficiency, speed and performance. It include the applications like low power CMOS, Quantum computer, Nanotechnology, Optical computing and self-repair.

In 2011, Md.Mazder Rahman et.al presented a quantum gate library that consists of all possible two-Qubit quantum gates which do not produce entangled states. These gates are used to reduce the quantum cost of reversible circuits. They proposed a two-qubit quantum gate library that plays a significant role in reducing the quantum cost of reversible gates.

In 2012, B.Raghu Kanth et.al described that implementing of reversible logic has advantages of reducing garbage outputs, gate count and constant inputs. Addition, Subtractions operations are realized using reversible DKG gate and it compare with conventional gates. The proposed reversible adder/substractor circuit can be applied to design of complex systems in nanotechnology.

In 2012, Mr. Devendra Goyal presented VHDL CODE of all Reversible Logic Gate, which provide us to design VHDL CODE of any complex sequential circuit. Here author have been tried to make the VHDL code as much as possible. Author can simulate and synthesis it using Xilinx software.

In 2013, Marek Szyprowski presented a tool for minimizing the quantum cost in 4-bit reversible circuits. Here Author shown that for benchmarks and for designs taken from recent publications it is possible to obtain saving in quantum cost comparing with existing circuits.

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In 2013, Raghava Garipelly Reversible logic is one of the most vital issue at present time and it has different areas for its application, those are low power CMOS, quantum computing, nanotechnology, cryptography, optical computing, DNA computing, digital signal processing (DSP), quantum dot cellular automata, communication, computer graphics. It is not possible to realize quantum computing without implementation of reversible logic. The main purposes of designing reversible logic are to decrease quantum cost, depth of the circuits and the number of garbage outputs. This paper provides the basic reversible logic gates, which in designing of more complex system having reversible circuits as a primitive component and which can execute more complicated operations using quantum computers. The reversible circuits form the basic building block of quantum computers as all quantum operations are reversible. This paper presents the data relating to the primitive reversible gates which are available in literature and helps researches in designing higher complex computing circuits using reversible gates.

In 2014, Ashima Malhotra et.al one of the most cited books in physics of all time, Quantum Computation and Quantum Information remains the best textbook in this exciting field of science. This 10th anniversary edition includes an introduction from the authors setting the work in context. This comprehensive textbook describes such remarkable effects as fast quantum algorithms, quantum teleportation, and quantum cryptography and quantum error-correction. Quantum mechanics and computer science are introduced before moving on to describe what a quantum computer is, how it can be used to solve problems faster than 'classical' computers and its real-world implementation.

It concludes with an in-depth treatment of quantum information. Containing a wealth of figures and exercises, this well-known textbook is ideal for courses on the subject, and will interest beginning graduate students and researchers in physics, computer science, mathematics, and electrical engineering.

PROPOSED MODEL:

In conventional (irreversible) circuit synthesis, one typically starts with a universal gate library and some specification of a Boolean function. The goal is to find a logic circuit that implements the Boolean function and minimizes a given cost metric, e.g., the number of gates or the circuit depth. At a high level, reversible circuit synthesis is just a special case in which no fan-out is allowed and all gates must be reversible.

The basic reversible logic gates encountered during the design are listed below:

NOT GATE:

The NOT GATE is the simple Reversible Logic gate. It is 1×1 Reversible Logic Gate with the quantum cost zero. The Not gate simply shifts the complementary of the input to output as shown in the figure. It is the basic primitive gate which may involve in construction of

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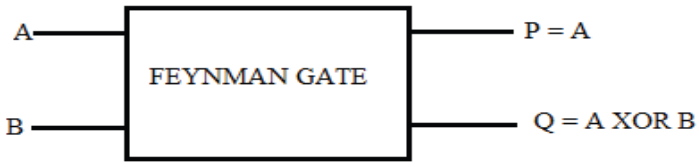
reversible logic gate, thus owing its own importance in determining the quantum cost of designed Reversible logic gate.

A	P
0	1
1	0

Fig. 1 NOT Gate and its Truth Table

Feynman Gate:

It is a 2x2 gate and its logic circuit is as shown in the figure. It is also known as Controlled Not (CNOT) Gate. It has quantum cost one and is generally used for Fan Out purposes.

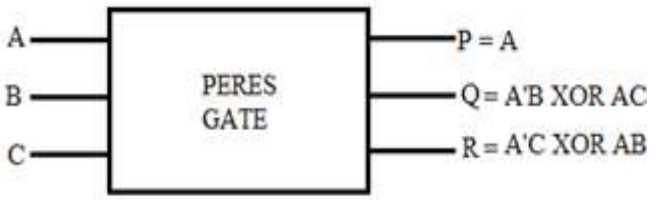


A	B	P	R
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

Fig. 2 Feynman Gate and its Truth Table

Peres Gate:

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost four. It is used to realize various Boolean functions such as AND, XOR.



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	0
1	0	1	1	1	1
1	1	0	1	0	1
1	1	1	1	0	0

Fig.3 Peres Gate and its Truth Table

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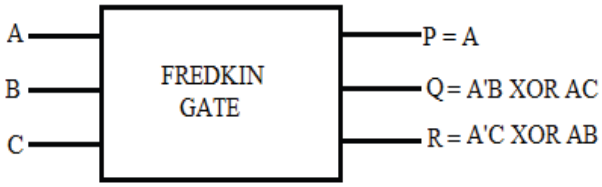
Fredkin Gate:

It is a 3x3 gate and its logic circuit is as shown in the figure. It has quantum cost five. It can be used to implement a Multiplexer.

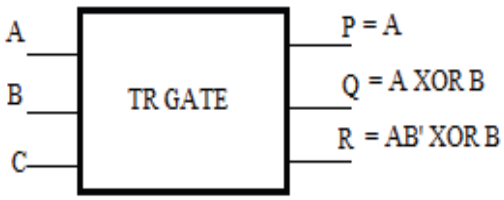


A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	0	0
1	0	1	1	1	0
1	1	0	1	0	1
1	1	1	1	1	1

Fig.4 Fredkin Gate and its Truth Table

TR GATE:

TR Gate is a 3×3 reversible gate. The outputs are defined as shown in the below figure7. The quantum cost of TRG gate is given by:



A	B	C	P	Q	R
0	0	0	0	0	0
0	0	1	0	0	1
0	1	0	0	1	0
0	1	1	0	1	1
1	0	0	1	1	1
1	0	1	1	1	0
1	1	0	1	0	0
1	1	1	1	0	1

Fig.5 TR Gate and its Truth Table

Considering our circuit requirements we need to design AND gate and OR gate using reversible gates. Here we used fredkin gate to design AND and OR gates as shown in figure. Importance is given to fredkin gate because it gives optimistic performance at less Quantum Cost for designing AND and OR gates.

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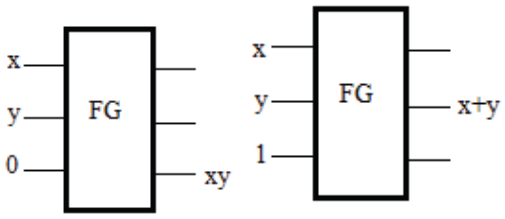

Fig.6 AND Gate using fredkin and OR Gate using fredkin

URG Gate:

The 3*3 Reversible gates with three inputs and three outputs. URG remains for Universal Reversible Gate. The inputs (A, B, C) mapped to the outputs is as appeared in Fig.7

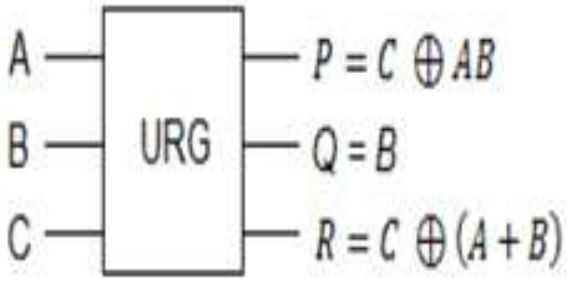

Fig. 7 URG gate

Machine gear-piece Reversible Logic Gates:

A 3×3 reversible gate COG (Controlled Operation Gate) as of now had been proposed [17] appeared in Fig. The nearer taking a gander at reality table uncovers that the input design corresponding to a particular output example can be interestingly decided and in this way be kept up that there is a one-to-one correspondence between the input vectors and the output vectors. In this gate the input vector is given by IV = (A, B, C) and the corresponding output vector is OV = (P, Q, R).

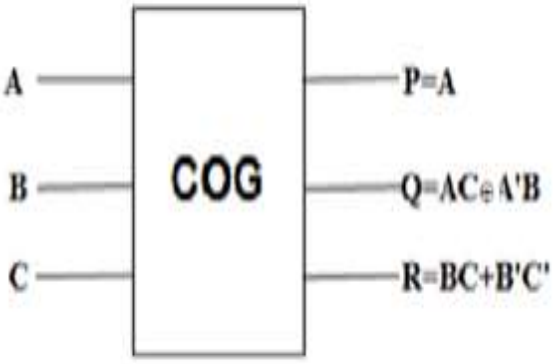

Fig. 8 COG reversible gate

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SBV Gate:

SBV gate is a 5 x 5 reversible gate whose fact table is as appeared in Fig.5. The Fig.6 demonstrates the proposed reversible logic gate which can exclusively work as a nine's complementary with one garbage output.

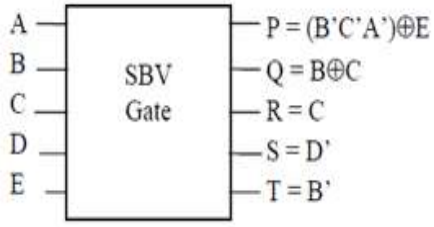

Fig.9 SBV gate

The proposed SBV gate can be utilized to acquire nine's complement of a number with E = 0. On the off chance that input number is B3, B2, B1, B0 whose 9"s complement is to be acquired then the outputs of SBV gate are as appeared in Fig.10.

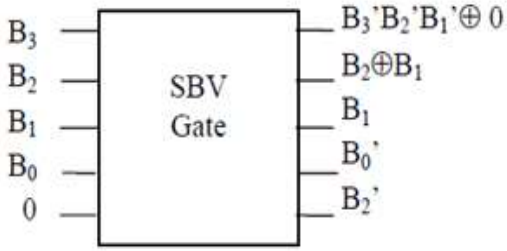

Fig. 10 SBV gate implemented as Nine's Complemented gate, where "B2" is a garbage

Output.

The reversible logic gates will be having n-input and n-output i.e. the meet number of input and equivalent number of output. In reversible logic, inputs can be remarkably recouped from the output. In the event that a reversible gate has k inputs, and therefore k outputs, at that point it is a k*k reversible gate. In reversible gates, fan out is not allowed, if there it must not surpass more than one. No criticism ways are permitted i.e. circuit is non cyclic. Some important factors in reversible logic are Garbage output, consistent input, quantum cost.

Gate Count (GC): It is the number of reversible gates used to understand the system.

Garbage Output (GO): It is the unutilized output from the reversible gate, it is especially basic to accomplish reversibility and it must be not utilized for facilitating calculation.

Consistent Input (CI): Constant inputs are those inputs that are utilized to create a given logical expression using the reversible logic gates. Steady inputs are kept up at either a consistent 0 or steady 1.

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Quantum Cost (QC): Each reversible gate has a cost related with it called quantum cost. The quantum cost of a reversible gate is the number of 2*2 reversible gates or quantum logic gates required in designing it. The quantum cost of all reversible 2*2 gates is taken as unity. The cost of all the 1*1 reversible gates, for example, the NOT gate is thought to be zero.

An effective design in reversible logic ought to have the accompanying highlights:

- Use the least number of reversible logic gates
- Should have less number of garbage outputs
- Less number of consistent inputs and
- Minimization of quantum cost.

RESULTS AND DISCUSSIONS:

Table III. Comparison between existing & proposed Write enabled master-slave D-FF

Write enabled master-slave D-FF	Comparison of cost		
	delay	Quantum cost	Garbage Outputs
Hafiz Md.2009[15]	25	25	7
Morrison 2011[16]	19	21	-
Proposed	16	16	3
Improvement w.r.t[15]	36%	36%	57%
Improvement w.r.t[16]	16%	24%	-

Existing outputs

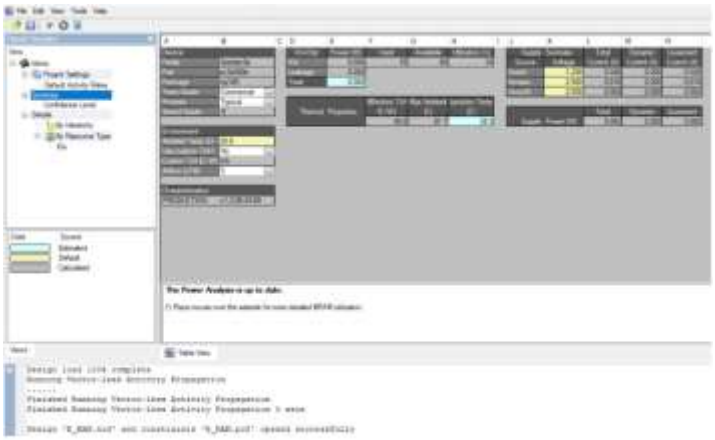

Fig. 11 Input Power to the gates

Above figure mentioned input value of the gates here we consider 25^{o} ambient temperature, power 0.082W

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Fig. 12 Delay

In above figure observed the delay of slices and input LUTs we are used 11 bonded IOBs and got delay 1.106

Fig. 13 Area

Observe the above figure the delay area and using gates of given project

Proposed outputs

Fig. 14 Power

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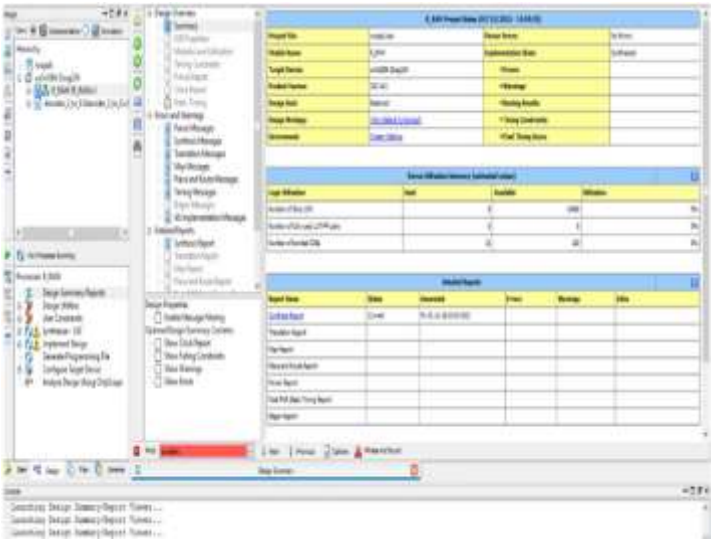

Fig.15 Delay

Figures 14 &15 given delay and input power of the proposed system compare to existing the utilization power was decreased 0.042W

Fig. 16 Area

Compare to existing method proposed system given better results and got the results 30%better

CONCLUSIONS:

A Reversible RAM may be considered as the brain of any computation and can replace the existing main memory in the forthcoming Quantum devices. In this work, we have shown a quantum cost efficient novel architecture of RRAM with the help of proposed MF gate, Reversible D-FF and decoder. Proper algorithms and lemmas have been mentioned for clarification of proposed design so as to have some idea about their efficiency. The architectures have been compared with the existing designs available in literature which corresponds to our success in terms of quantum cost, ancilla and garbage. We have addressed about the worst case delay (logical depth) which has hardly been done earlier. The novel reversible realization and optimization of RRAM will play a big role to reversible logic

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community to work further for the design of a synchronous N-bit dual-port SRAM array and DRAM array for their application in FPGA or Network-on-chip.

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REFERENCES:

1. R.Landauer, "Irreversibility and heat generation in the computational process", IBM Journal of Researh. Dev. 5, 183-191, 1961.
2. C.H.Bennett, R.Landauer, "The fundamentals physical limits of computation".
3. C.H.Bennett, "Logical reversibility of computation", IBM Journal of Research. Devel. 17, 525-532, 1973.
4. Tommaso Toffoli, "Reversible Computing," Automata, Languages and Programming, 7th Colloquium of Lecture Notes in Computer Science, vol. 85, pp. 632-644, 1980.
5. E. Fredkin, T.Toffoli, "Conservative logic", Int. J. Theor. Physics 21, 219-253,1982.
6. A Peres, "Reversible logic and quantum computers", Phys. Rev. A, Gen. Phys. 32, 6, 3266-3276,1985.
7. P. Picton, "Multi-valued sequential logic design using fredkin gates" MVL 1. 1,241-251,1996.
8. J.Smolin, DDivincenzo, "Five 2-bit quantum gates are sufficient to implement quantum Fredkin gate", Phys. Rev. A 53, 2855-2856,1996.
9. H. Thapliyal, M. B, Srinivas, M Zwolinski, A beginning in the reversible logic synthesis of sequential circuits. In Proceedings of the Int. Conf. on the Military & Aerospace Programmable Logic Devices. 2005.
10. Rice, "A new look at reversible memory elements", In Proceedings of the International Symposium on Circuits and Systems. 243-246, 2006.
11. H. Thapliyal, A P. Vi nod, "Design of reversible sequential elements with feasibility of transistor implementation'" In Proceedings of the IEEE international Symposium on Circuits and System, 625-628,2007.
12. 1. Rice, "An introduction to reversible latches", Computation. 1. 51, 6, 700-709, 2008.
13. M.L. Chuang, C. Y. Wang, "Synthesis of reversible sequential elements" J. Emerg. Techno!. Comput. Syst. 3,4,1-19,2008.

ISSN PRINT 2319 1775 Online 2320 7876

Research paper **© 2012 IJFANS. All Rights Reserved,** UGC CARE Listed (Group -I) Journal Volume 11, S Iss 2, 2022

14. K. Morita, "Reversible computing and cellular automata-a survey", Elsevier Theor. Comput. Sci. 395, I, 101-131,2008.

15. Hafiz Md., Md. M.A.Polash, AS. Md. Sayem, "A novel design of a reversible field programmable gate array", Silver Jubilee Conference on Comm. Tech. & VLSI Design(CommV09), VIT University, Veil ore, India. Oct 8-10,2009, pp 502-503.

16. Matthew Morrison, Matthew Lewandowski, Richard Meana and Nagarajan Ranganathan, "Design of Static and Dynamic R AM Arrays using a Novel Reversible Logic Gate and Decoder" 11 th IEEE Int. Conference on Nanotechnology, Oregon, USA, August 15-18, 2011.

17. Sic Noor Mahammad and Kamakoti Veezhinathan, "Constructing Online Testable Circuits Using Reversible Logic", IEEE transactions on instrumentation and measurement, vol. 59, no. I, January 2010.

18. AK. Biswas, "Eflicient Design of N-bit Reversible Processor" B.Sc Thesis, University of Dhaka, Bangladesh, 2008.

19. Abu Sadat Md. Sayem, Masashi Ueda, "Optimization of reversible sequential circuits", Journal of Computing, Vo!.2, Issue.6, June 2010.

20. H. Thapliyal and N. Ranganathan, Design of Reversible Sequential Circuits Optimizing Quantum Cost, Delay, and Garbage Outputs, ACM Journal on Emerging Technologies in Computer Systems,Yol. 6,No. 4,Article 14, Pub. date December 2010.

21. L. Jamal, F. Sharmin, Md. A Mottalib and H.M.Hasan Babu, "Design and Minimization of Reversible Circuits for a Data Acquisition and Storage System", Int. Journal of Engg. & Tech. Vol.2 No.1, Jan 2012.

22. Mohammadi,M. and Mshghi,M, On figures of merit in reversible and quantum logic designs, Quantum Inform. Process. 8,4,297-318,2009.

23. Michael A Nielsen, Isaac L. Chuang, "Quantum Computation and Quantum.

24. P Ashok Babu, V Siva Nagaraju, Ramya Mariserla, Rajeev Ratna Vallabhuni, “Realization of 8 x 4 Barrel shifter with 4-bit binary to Gray converter using FinFET for Low Power Digital Applications” , Journal of Physics: Conference Series.

25. Dr. P Ashok Babu, “ An Implementation of Area Optimized Low Power MAC”, Journal of Mechanics of continua and Mathematical Sciences, Vol.14, No.3, PP: 112-123.