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ANALYSIS ON THREE-PHASE, THREE-LEVEL T-TYPE CONVERTER DESIGN AND IMPLEMENTATION FOR GRID APPLICATIONS

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ABSTRACT
In order to guarantee adequate power quality for low- and medium-power dc to ac energy conversion applications, multilevel inverters (MLIs) have emerged as the go-to technology. The MLIs have a variety of benefits over conventional two-level inverters, as well as a lower dv/dt, reduced electromagnetic interference, as well as the capacity to knob better voltage levels by apparatus through a lower voltage rating. Now the properties contain expanded the appeal of a range of industrial uses, including in movements, mixers, marine effort, reactive power correction, and the conversion of renewable energy. This research was motivated by the requirement to create a large amount of voltage levels though preserving the maximum practicable level of circuit dependability. A new topology is therefore developed using the fundamental MLI setups, specifically three phases T Type converter is projected here**.**
Keywords: T-type converter, high efficiency, three-level converter

1. INTRODUCTION

Energy conversions in the low voltage area have recently attracted a lot of attention. Examples of applications include photovoltaic grid inverters, PFC rectifiers, and automotive inverters. Structure utilizing inverters must be both affordable and highly efficient must have inexpensive, tiny passive components. The efficiency suffers as a result of the switching frequency being repeatedly amplified to the medium level assortment of 12–25 kHz, that results in larger switching losses. structure performance another issue is acoustic noise. Do not try to reduce acoustic noise necessary in high-speed drives and aviation application. Elevated control and output frequencies able to 1 kHz are common. There is a demand for bandwidth. The exchange is finished here. According to earlier studies, multilevel topologies with high degree of complexity has effectiveness of the converter has a flat relationship with the switching frequency [1], [2] The current research illustrates the aggressiveness of the 3-level T-type converter (3LT2C) in low-voltage determinations. Evaluated by three-level NPC design, the T-type topology has an active bi-directional switch at the dc-link voltage midpoint and uses2less diodes per bridge leg. Its three-level construction is simpler than that of active neutral point clamped converters [9]–[11] or split-inductor converters [12, [13]. The 3LT2C integrates the benefits of two-level converters, like reduced conductivity losses, a tiny part count, and an intuitive operating principle, by the benefits of three-level converters, for instance decreased switching losses and higher output voltage consistency. If a two-level voltage source converter is used, A three-level (VSC) construct by 1200-V IGBTs is assessed using a VSC improvedby 1200-V IGBTs. The effectiveness of the three-level converter could differ improved by neutral point clamped (NPC) converter is designed by 600-V devices. Because of reduced conduction losses and elevated efficiency, Because of the3LT2C's minimal switching losses, it has a high efficiency. High, especially for switching frequencies among 8 and 24kHz) in industry, term is frequently used. This is done without the use of SiC devices, which can be exceedingly expensive if the choice of chip size results in equal conduction losses. The 3LT2Cisseenas a viable option to two-level converters for low-voltage applications where improved efficiency is required.

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Having high switching frequency and efficiency is a crucial goal.

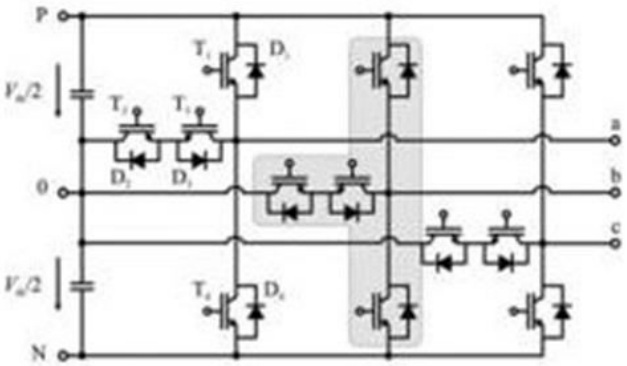

Figure 1:.The three-level T-type topology be representing here illustrated. An vigorous, bidirectional switch is added by dc-linkmid point, extending the traditional two-level VSC design. The T-type VSC's single-bridge leg mimics the figure of the turn around quality "T," hence the topology is called T-type topology.

2. LITERATUREREVIEW

In the last decade, multilevel inverters have gained popularity in academics and business for controlling high- and medium-voltage energy. Furthermore, evaluated to a two-level converter by a comparable rating, they can produce switched waveforms by lower harmonic distortion. By using many layers, it is possible to eliminate harmonic distortion while maintaining a steady inverter power output. In multilayer topologies, the association among the converter effectiveness and switching frequency is very flat.

A three-level neutral point clamped (NPC) conversion by 600-V devices may be more efficient than a two-level voltage source converter (VSC) through 1200-V IGBTs. When differentiated to the three-level NPC configuration, the T-type topology demands2few diodes per bridge leg and only a single active bidirectional switch at the dc-link voltage midpoint.

Its three-level construction is less complex than that of split-inductor converters or active neutral point clamped converters. The 3LT2C combines the benefits of two-level converters, like reduced conveyance losses, a minimal part count, and an intuitive process method, with the benefits of three-level converters, like decreased switching losses and higher output voltage quality.

3. METHODOLOGY

THE T-TYPETOPOLOGY

In outline 1, the 3LT2C's basic structure is displayed. 1. The conventional two-level VSC prototype is improved by the inclusion of an active, bidirectional switch at the dc-link halfway point. In low-voltage situations (here $Vdc = 650\ V$, for instance), the entire dc link voltage has to be restricted which is why the high side and low side switches ($T1 / D1$ and $T4 / D4$) are usually employed with $1200 - V$ IGBTs/diodes. Yet, the bidirectional switch leading to the dc link midpoint only needs to prevent 50% of all dc link power. The present instance makes use of2anti-parallel $600 - V$ IGBTs, although it may additionally be constructed using lower-voltage components. [cf. Fig. 2(a)]. The centre switch contain suitable conductivity losses and extremely low switching losses due to the decreased obstruction voltages, even though it is coupled in series with2other devices the other switches.

Compared to the three-level NPC approach here is no series connection of devices present that must block the entire Vdc of the dc-link. Since it's a chance that an incompatible component of the voltage could become prohibited in the impermanent scenario whereas both IGBTs attached in series turn off concurrently, switching transitions about the positive (P) to the negative (N) dc-link voltage level and inversely must be carefully considered, which is a step that is usually skipped in the NPC topology. This undesirable impact is not conceivable with the T-type topology. Low-level algorithms that enable transient voltage balancing between series linked IGBTs or stop such transitions are not required.

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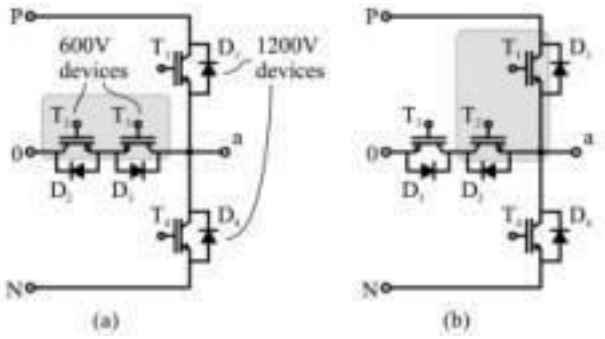

Fig2: Using 2IGBTs in a common emitter or common collector arrangement, a directional switch can be built to the middle.

Reduced conduction losses are another advantage of utilizing solitary 1200-V procedure to obstruct the whole dc link voltage when bipolar devices are used. When the yield is associated to (P) or (N), Only one device suffers a forward voltage drop, but two devices are always present in the NPC topology. associatedinseries.The3LT2C's conductivity losses are significantly decreased, building it a viable option yet for low switching frequencies.

The initial purpose of the three-level NPC topology is meant for medium-voltage applications. The devices had to be connected in series because of the low voltage blocking capabilities of the devices that were available. The expanding voltage handling capacity and the straightforwardly associated increases the power handling capacity outweighed the disadvantage of amplified conduction losses caused by series-connected bipolar devices. On the other hand, low-voltage applications don't need this benefit. Because the current devices have adequate voltage ratings and quick switching rates, connecting them in series is not required. Increased phase currents result in increased output power.

Conduction losses area significant limiting factor in ideally, they should be kept as low as practical within the power range. The T-type topology is consequently employed. The T-type architecture is also referred to as a neutral point piloted (NPP) converter or a transistor clamped converter in medium-voltage applications [14], [15]. (TCC). In medium voltage applications, a single device's voltage blocking capabilities are insufficient to obstruct the entire dc-link voltage. It is necessary to swap out the switches T1 and T4 with a two-IGBT series connection.

Energetic gate drive units are essential for temporary and steady-state voltage balancing.

Conduction losses rise and the implementation effort is greatly increased as a result of bipolar devices being connected in series. As a result, this setup isn't suggested for low-voltage applications.

4. SWITCHARRANGEMENT

The 2660 V IGBTs can be linked in a common emitter configuration or a common collector configuration to form a bidirectional switch. In compared to the two-level VSC design, the combined emitter configuration [cf., Fig. 2(a)] necessitates three extra gate drive supplies, or an additional isolated gate drive supply voltage.

If a common collector conformation is used [see Fig. 2(b)], is utilized, this number can be lowered even further. T2 now shares an emitter with T1 on the topside and is powered by the isolated gate drive voltage of T1.Themidpoint voltage level is connected to the second 600-V IGBT's emitter. Although the 3-phase topology is fully explained, all three IGBTs (T3, a, b, and c) split a common emitter, necessitating an immediate requirement for a single inaccessible gate drive supply. Comparing to the two-level configuration, the entire T-type topology might have been achieved with one more unreachable gate drive supplies.

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TABLE I
SWITCHING STATES

State	V_{out}	T_1	T_2	T_3	T_4
P	$+V_{dc}/2$	on	on	off	off
0	0	off	on	on	off
N	$-V_{dc}/2$	off	off	on	on

The inaccessible gate drive provide of the high-side switch T1 does not require a higher power rating if the gate incriminates of the 600 and 1200-V IGBTs are roughly equivalent. Due to the established commutation and modulation method, as shown in the next section, T1 and T2 are newly switched in the same modulation cycle. The cost will be slightly increased by the need for an additional six gate drive ICs and six digital isolators for the switch signals.

The clamping diodes are eliminated in comparison to the three-level NPC topology, lowering the necessary number of diodes from 18 to 12. Additionally, the change from six to one isolated gate drive supplies is a significant improvement that can help reduce costs.

5. COMMUTATION

For the 3LT2C, the switch commutation must be carefully examined. As shown in Figure 3, the amount produced of abridge support could exist linked to the positive (P), neutral (0), or negative (N) dc-link voltage level. For all current directions, closing T1 would result in a positive voltage level, closing T2 and T3 would result in a neutral voltage level, and closing T4 would result in a negative voltage level. This technique, however, would necessitatea present- dependent commutation progression. Fortunately, this simpler commuter strategy works regardless of the current orientation.

If T1 and T1 and T2 are both closed The current trajectory will consequently convert to the precise branch regardless of the current path for the positive voltage level, T2 and T3 for a neutral voltage level, and T3 and T4 for the negative voltage level. Table I lists the switches that must be closed in sequence to attain the coveted output voltage. To prevent a dc-link short circuit, all switches only need a simple turn-on delay. The modulation of these switch signals is identical to the modulation of the three-level NPC topology when worn The output phase of the positive output current in Fig. 3(a), whose T1 and T2 are stopped, is associated to the positive (P) voltage level. Subsequent to the turn-on delay, T3 is terminated, and T1 is opened to commutate to the nonaligned level (0).

When T1 is turned off, the present commutates obviously over T2 and D3 to the neutral level. The current commutates to the impartial for a negative phase current when T3 is closed [see Fig. 3(b)]. T1 is stopped following the turn-on delay when we transition from (0) to (P), followed by the opening of T3. A positive phase current that is flowing through D3 when T3 is off [see Fig. 3(c)] change to the positive voltage level when T1 is turned on. When T3 is turned off, the current for a negative phase current change to D1 [see Fig. 3(d)].This principle applies to all other switching transitions.

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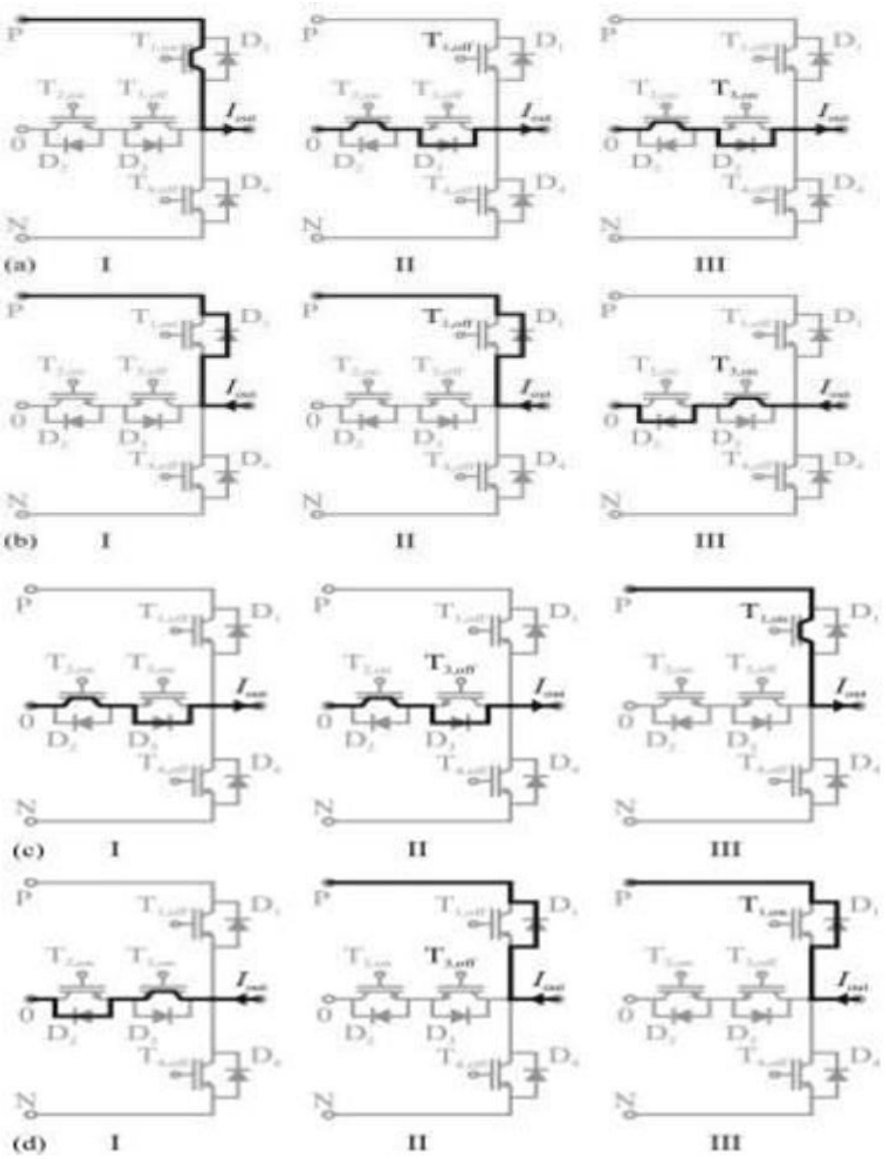

Fig3: present commutation throughout the switching transition for both (a) positive and (b) negative output current (P 0). Commutation of current for the (c) positive and (d) negative output currents during the switching transition (0 P)

Since space-vector intonation only happens at sector borders, direct transitions as of (N) to (P) and inversely are let alone. The 600-V diodes experience higher losses as a result of the switch, while the 3LT2C is unaffected. The blocking voltage transition from -Vdc/2 to +Vdc/2 via D2 and D3 causes an invalidate improvement current pulse to flow to the neutral voltage level. Additional losses in the diodes are attributable to the reverse revival current.

The modulation cycle in which the IGBTs T1 and T2 are switched is different cycle because through transitions as of (N) to (P) and inversely are present. As a result, as stated in Section II-A, If the higher end of switch T1's sequestered gate drive supply is utilized to power the gate drive part of T2, the necessary electrical consumption is not increased.

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SIMULATION

A simulation and experimental tests were undertaken to test the T-type three level PWM converter's neutral point current analytical model that was obtained. Three phase grid voltages used phase locked loops (PLL) to calculate the phase angle and frequency of grid. The characteristics of the absolute method are given in Table 2.

TABLE2.SYSTEMPARAMETERS

PARAMETERS	VALUE
Grid voltage	22KV
Rated power	20MVA
amount of H bridge per phase in shunt	18
amount of H bridge per phase in series	10
Line reactance	0.31H
Source reactance	35Mh
Shunt reactance	0.31H
Rated frequency	50Hz
Sampling frequency	2500Hz
Line current	100amp

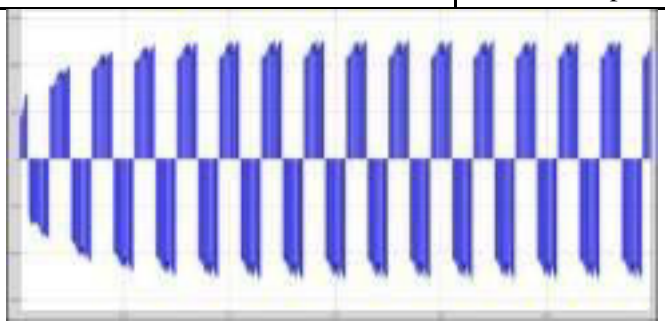

Fig4: Output phase voltage

Fig4demonstrates the voltage in the inverter phase. These are the three levels: P, O, and N. The data in table 2 and this waveform are equivalent. This graphic demonstrates the dc-link capacitor voltage's volatility. This is due to dc bus capacitor voltage being unbalanced.

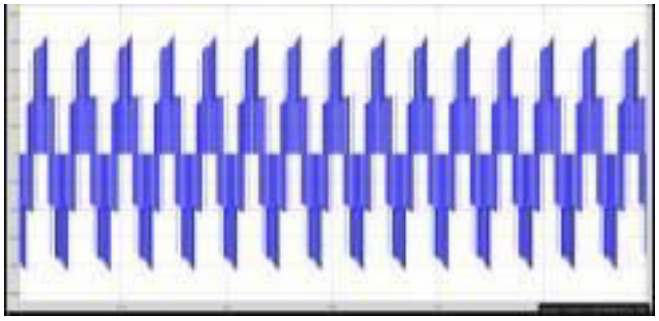

Fig5: Output line voltage

The inverter line voltage is revealed in Fig. 5. There are five levels total. The harmonic content of this voltage waveform is significantly lower by a conventional two-level inverter operating at the similar

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switching frequency. The DC link when voltage is extremely high or the grid voltage is extremely low, the waveform may only have three levels.

Fig 6: Filtered line voltages

Fig 6 shows filtered line voltages. It is displayed for each of the three voltages. A filter was used to make these waves

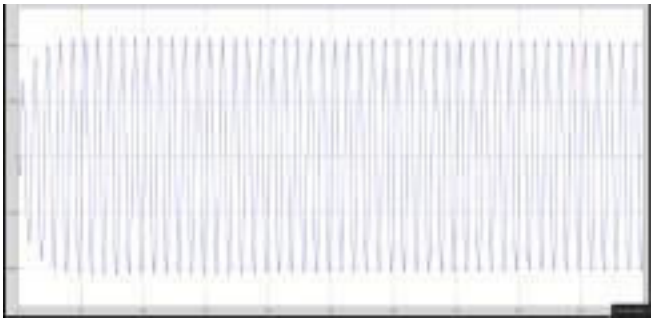

Fig 7: Line currents

Fig7 depicts the three line currents that are in phase and amplitude as expected.

CONCLUSION

In this work, the 3LT2C was developed for applications requiring high effectiveness at low voltage. Here two-level VSC resolution on behalf of medium switching frequency applications and it works best between 4 and 30 kHz. The key benefit is a lower commutation voltage that diminishes switching losses in comparison to a two-level system. There aren't many differences in the conduction losses.

An anti-serial bidirectional switch in the dc-midpoint connector is studied using2600-V IGBTs in common-emitter or common-collector setups. Also demonstrated were the benefits of the common-collector option's additional isolated gate drive supply. A simple commutation strategy that is unaffected by the present direction be developed. The loss of the 3LT2C is calculated using a method that fails to consider the loss optimal clamping method and the temperature dependence of the loss components. The expected efficiency of 98% was confirmed by measurements performed on a 10-kW unit of the 3LT2C.

REFERENCES

1. "A comparison of three-level converters to two-level converters for low-voltage drives andutilityapplications," IEEE Trans. Ind. Appl., vol. 41, no. 3, pp. 855–865, May 2005.
2. Schweizer.M,Friedli.T, and J. W. Kolar, “Comparison and implementation of a three-levelNPC voltage dc linkback-to-back converter with Sic and Si diodes,” in Proc. IEEE 25th Ann. Appl.Power Electron.Conf.Expo.,pp.,1527–1533.
3. A.Nabae,I.Takahashi,"NeutralpointclampedPWM"IEEETrans.Ind.Appl.,vol.IA-17,no.5,
4. September1981,pp.518–523
5. Joetten.R,Gekeler.M,"ACdrivewiththree-

levelVSCandhighperformancemicroprocessorcontrol,"inProc.Eur.Conf.PowerElectronic.Appl.,Belgium, October.1985,pp.3.1–3.6

6. B.Fuld,"Comparaitive evaluation of modern 3-level inverter" in etzArchiv, vol. 11, Berlin:VDEVerlag, Germany1989,pp.261–264.
7. T. Takeshita and N. Matsui, "PWM control and input characteristics of three-phase multi-levelAC/DCconverter," IEEE 23rd Annu. Power Electron. Spec. Conf., pp. 175–180, 1992
8. T. Bruckner, S. Bernet,and H. Guldner, "The active Neutral Point Clamped converter and its loss balancing control," IEEE Trans.Ind. Electron., vol. 52, no. 3 (June 2005), pp. 855–868.
9. "Advanced three-level topology withcomponents: Properties and control mechanisms," in Proc.IEEE 35th Annu. Conf. Ind. Electron. Soc.,2009,pp.676–681.J.
10. Li, J. Liu, D. Boroyevich, P. Mattavelli, and Y. Xue, "3-level active npc zero-current-transitionconverter for sustainable energy systems," IEEE Trans. Power Electron., vol. 26, no. 12 (December 2011),pp.3680–3693.
11. V.Peron-Guennegues,C.Conilh,andL.Leclere,"Aconvertertopologyforhighcurrentdensitydriveapplications,"inProc.14thEur.Conf.PowerElectron.Appl.,pp.1–8
12. I.Baraia,J.Barrena,G.Abad,J.CanalesSegade,andU.Iraola,"Anexperimentallyprovenactivegatecontrol approach for the series connection of IGBT/Diodes," IEEE Trans. Power Electron., vol. 27, no. 2,pp.1025–1038,February2012..
13. [13] R. Withanage and N. Shammas, "Series connection of IGBTs," IEEE Trans. Power Electron., vol. 27,no.4(April2012),pp.2204–2212.